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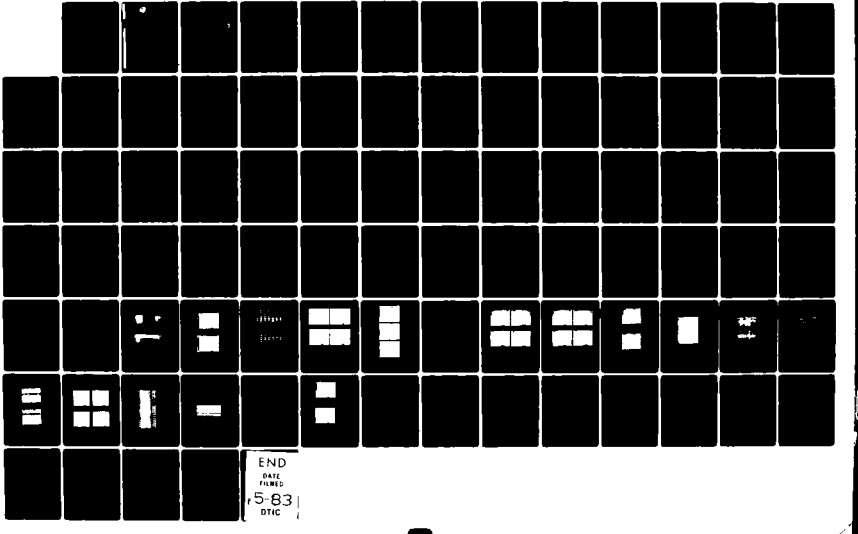

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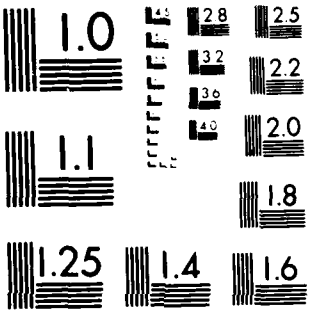

The Acquisition of Development of Advanced Processing Techniques for CCD Arrays

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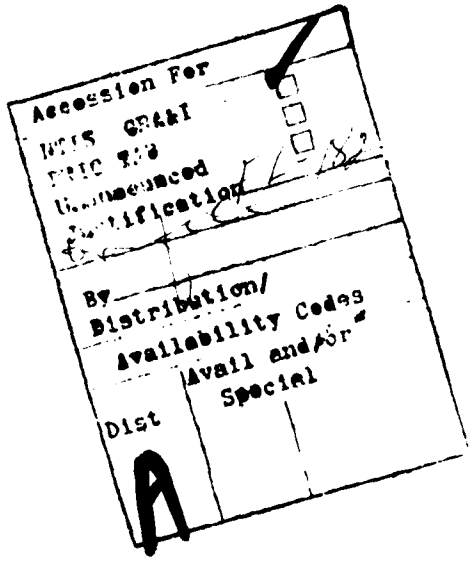

FINAL REPORT

The Acquisition of Development of Advanced Processing Techniques for CCD Arrays

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1. INTRODUCTION

The program of work ~~in DARPA Contract # MDA 903-81-C-0390~~ involves two major tasks. The first task includes the design and fabrication of a TDI test mask for evaluation of potential design and processing improvements to TDI imagers. The second task investigates materials and process research topics aimed at improving processing techniques suitable for large imagers.

The DARPA Contract has been successfully completed and this final report presents the results of both tasks. The first task is presented in Sections 2-5 while Sections 6-9 describe the results of the second task. The conclusions and suggestions for future work are presented in Section 10 and 11, while Section 12 acknowledges those involved in successfully concluding this work.

2. DESIGN OF W66A, THE TDI TEST MASK (TASK 1 - PART A)

The development of charge coupled device imagers is proceeding at a rapid pace as a result of the excellent imagery and performance versatility of these electro-optic sensors.

The time delay and integration (TDI) mode of operation is necessary in certain imaging applications where there is a large linear motion, with respect to the focal plane, of the scenery to be imaged during the integration period. In this mode of operation, the line imagery formed from a scene is clocked from a linear array to an adjacent linear array to compensate for the image motion. The effective exposure time can thus be increased many times over that of a linear array without causing smearing in the imagery. The TDI mode of operation provides superior signal-to-noise ratio and is particularly useful for low light level imaging applications.

A continuous array of several TDI imagers can be formed by mounting buttable CCD imager chips end-to-end with all connections made through the non-buttable sides of the chip. With this approach, a very long focal plane array can be formed without being limited by the physical length of individual imager chips.

The TDI test mask, known as the W66A, is a monolithic CCD imager test chip designed specifically for the evaluation of buttable TDI imager design modifications and new processing techniques for improved imager performance. Design modifications may be unambiguously evaluated by comparing "redesigned" imagers with "standard" imagers on-chip, hence eliminating the uncertainties of various process variables that occur from wafer-to-wafer and batch-to-batch.

The design description has been repeated in a mid-term report prepared for DARPA under the same contract and is included here as Appendix I. Basically, the mask includes three TDI imagers that are nearly identical.

One of these imagers, W66A-HSC, is used as a "standard" to allow isolation and identification of problems other than those resulting from design modifications. The other two imagers, W66A-HSB and W66A-HSA, include the necessary design changes. The "A" and "B" devices are compared on-chip to the standard device, "C", for unambiguous electro-optical performance data. Figure 1 depicts the design organization of the W66A test chip. Various BNR/NTE test inserts generated on the same mask are not considered in this report. The block diagram of the 512 X 96 buttable TDI imager is shown in Figure 2. Figure 3 shows details of the redesigned buttable edge circuitry. Further information is contained in Appendix I.

3. W66A PHOTOMASK PROCUREMENT

The W66A mask set was generated internally and photomask procurement was generally standard as per the GCA DSW 4800 Wafer Stepper specifications[3]. However due to stringent design rules required for the adjacent BNR Test Insert Chip[4] two different biases had to be used at the contact level stage. The total mask set includes 10 levels. Pyrox 2 and Metal 3 levels have not been generated. The mask set is made for positive resist processing of wafers and includes the Wafer Stepper alignment marks. The total number of devices per 100 mm diameter wafer is 78, i.e., 234 single imagers altogether.

4. W66A WAFER FABRICATION

Two batches, JE07A and JE08A, were processed for this task. The major aim for processing these two batches was to verify the design modifications.

The first batch, JE07A, was processed with the standard BNR double-poly, double-metal, buried-channel CCD process. Only wafers #1-10 of this batch are covered by the DARPA contract. The standard process is the one used for the ITEK E57B 96 x 2048 TDI imager production run. A minor change was incorporated on wafers #1-3; an *in situ doped-polysilicon* technique was used instead of the standard polysilicon step. The complete process matrix for this batch is shown in Figure 4 and is basically intended for

(i) Testing design modifications.
(ii) Testing the in situ doped-polysilicon process.
(iii) Verifying chemical etch techniques for the butting process.

Problems were encountered during fabrication of these batches which resulted in severe delays of the completion date. The first problem was a wafer cleaning problem which was traced to a specific source of contamination. Another major problem was encountered during the Metal 2 photoengraving step of Batch JE07A. During the Metal 2 etch it was observed that the Metal 1 layer was attacked in various locations. It has been assumed that this was the result of pinholes in the Pyrox 1 layer.

A severe shorting problem was observed between the Metal 1 and Metal 2 electrodes on all wafers during testing. This precluded the derivation of any meaningful information from Batch JE07A.

The process matrix used for the second batch, JE08A, is shown in Figure 5. Again, only 10 wafers of this batch are covered by the DARPA Contract. This batch was intended for

(i) Testing design modifications.

(ii) Testing the effects of the compensation implant dose on saturation levels, MTF and general dark current.

(iii) Investigating possible benefits of incorporating a compensation implant anneal.

5. ELECTRO-OPTICAL TEST RESULTS FOR W66A

5.1 Test Results for Batch JE08A (Batch 2)

Processing of this batch was devoid of major problems and subsequent testing indicated a high percentage of working wafers. From the significant numbers of all three TDI structures that were found to operate correctly on each wafer, one can deduce that the W66A mask design was implemented correctly at all stages. The test results are presented individually for the sake of clarity.

5.2 Redundant Bonding Pads (Device W66A-HSB)

The bonding pad area was increased from 125 microns x 125 microns to 140 microns x 250 microns to make a large enough pad area for multiple die probing at the wafer stage and reliable die bonding at the packaging stage (Figure 6). No problems were encountered with the present approach and a significant area of virgin metal remains for subsequent die bonding (Figure 6b).

5.3 Addition of Input Protection Devices (Devices W66A-HSA, -HSB)

The addition of input protection devices was prompted by ESD breakdown problems that were observed on earlier ITEK designs during sawing and handling. To prevent destructive failure a standard protection device based on an RC network with associated diode shunts was incorporated on isolated polysilicon gates. Care must be taken not to forward bias these N+ diodes. To prevent any spill-over of charge from or into the shift register, it has been customary to bias the shift register input gate, $\emptyset_{ISR2}$, at -5V while the substrate was biased at -3V. Although this is no longer possible on the A and B devices a new set of optimum operating voltages apply (Table IV) without any noticable deleterious effects to device operation. Output signals for A, B, and C devices (on same chip) were carefully compared to determine whether the addition of the RC protection circuit

would degrade the maximum frequency of operation. All devices were probe tested at a master clock frequency of 6-8 MHz, an upper frequency limit which is dictated by the cable and proper capacitance. No deleterious effects, such as signal rounding, were noticeable on any of the devices. The wafers were then sawn, and selected die individually separated and packaged.

To evaluate the breakdown characteristics of the protection devices the input gates on A, B, and C devices were investigated both with a curve tracer and an ESD generator. The curve tracer showed that the unprotected gates break down at approximately 60V while the protected gates break down at approximately 70V, and sink 70 mA. When the ESD generator was used the protected gates withstood repeated static charges of 550 $\pm$ 50V before destructive breakdown while the unprotected gates were destroyed by static voltages less than 100V.

The ESD generator used was an ANDY HILL Associates, MODEl ESD254. It has an internal RC circuit consisting of a 150 pF capacitor and a 1 Kohm series resistor to simulate the human body.

5.4 Redesign of Mid-output and End-Output to Remove the Split Video Level (Devices W66A-HSA, -HSB)

A split output video level was observed on the ITEK E57B device and was traced to capacitive coupling between the $\emptyset_{C1}$ clock and the output node diffusions[1]. The split level on the mid-output and end-output is caused by two different capacitive coupling paths. Both outputs were redesigned to reduce/eliminate this coupling on the High Resistivity W62A imager, and the same redesigned outputs were implemented on the A and B devices.

Figure 7a and 7b show the resulting waveforms at the mid-output and the end-output respectively. The split video level is removed completely at the mid-output. An unavoidable 10 mV split level still exists at the end-output corresponding to a $\emptyset_{C1}$ clock voltage = 18 V. It is not immediately

apparent at this stage whether with the utilization of a Metal 3 level this split video level can be reduced further.

Significant rounding of the mid-output signal is evident from Figure 7a. The reason for this is undetermined as yet. This may present a premature limit to the maximum frequency of operation of the mid-taps.

5.5 Reduction of $\emptyset_{1L}$ Shadowing (Device W66A-HSB)

The shadowing of the E1 sensing electrode in this region is believed to be a result of two factors.

The major factor is caused by a Poly 2 access tab running over the E1 sensing electrode to connect with the $\emptyset_{1L}$ electrode, Figure 8a. This Poly 2 tab shadows the E1 electrode reducing the quantum efficiency in this local region by approximately 33%. This connection tab has been reduced from 12 um to 5 um in the redesigned version, Figure 8b, reducing the effective shadowed region by 50%. It is doubtful whether any further reduction may be achieved with the present technology.

The second factor is due to the alignment tolerance (misalignment) of M2 to M1 shields. Since M1 has to contact the Poly 2 tab described above, the optical shield in this region has to be designed with M2. This factor is very significant on the E57B imager because the M2 region extends over 3 pixels and, with the inherent registration and etching tolerances between the two metal layers realized with contact aligners and negative resist, an apparent difference in sensitivity, with respect to nominal, is observed over this 3 pixel region. On the W66A-HSB device the M2 to M1 misalignment is approximately 0.1 um, due to the use of a stepper and positive resist, and this effect is hardly noticeable. In future, a M3 shield would eliminate this factor completely.

The test results for the odd- and even-interlace video outputs are shown in Figure 9. It is noted that the shadow effect is reduced from 45 mV (Figures 9a, 9b) to 20 mV for the redesigned version (Figures 9c, 9d). The effect of M2 to M1 misalignment is barely noticeable.

5.6 Reduction of the High (25V) Reset Voltage (W66A-HSB)

The enhancement mode reset transistor has been replaced by a buried channel transistor as was the case with the earlier ITEK 735A imager. Figure 10a, b shows the standard HSA device operating with reset voltages of 25V and 15V respectively. The device fails at low reset voltages. Figure 10c shows the redesigned HSB device operating correctly with a reset voltage of 15V. Use of a depletion reset MOST results in a decrease in signal level from 240 mV (Figure 10a) to 200 mV (Figure 10c). This 20% signal reduction is due to the increase in the overall capacitance of the output node diffusion because of the additional capacitance associated with the buried channel of the reset transistor. The situation is depicted schematically (pictorially) for both the enhancement and reset transistors in Figure 11.

5.7 Equalization of the E1 Mode Optical Window Size of the E1 Electrode

After a careful study of all relevant factors involving E1 optical window equalization it was decided that no design change should be effected in this regard. The E1 optical window is 12.5 um wide while the other TDI electrodes are 13 um wide. The small reduction in the optical window size is meant to compensate for variation in the optical sensitivity due to structural differences. The E1 window width for the A, B, C devices is the same.

5.8 Buttable Edge Redesign (Device W66A-HSA)

This was a major redesign feature incorporated on the HSA device only. Basically, it allows for a N+ diffusion guard band to completely surround the imagers. For the E57B this guard band is absent from the shift register input and output regions because of extremely tight geometries. To achieve this design feature the design rules would have been violated. The absence of a guard band results in the collection of spurious charge in the first and last set of pixels effectively degrading the device. This signal collection is usually noticeable in pixels #1 and 2 and pixels #2046, 2047,

and 2048. In some cases charge collection extends beyond these pixels. The excess signal is measured here as a percentage (Table I) of the signal in pixels sufficiently far from the edge. Measured values ranged from a minimum of 0% to a maximum of 150%. Intensive testing of the HSA and HSB devices indicate that incorporating the redesign feature helps reduce the amount of collected charge. Further, yield figures suggest that, utilizing the DSW 4800 wafer stepper and a positive resist process, this design feature may be successfully implemented.

Unfortunately, this feature has not been tested for devices where the buttable edges are achieved by chemical etching. Such work was intended to follow from Batch 1.

Detailed comparisons between the HSA and HSC devices were made by photographically recording video signals of the input and output edge pixels before and after saw cutting. The saw cut distance is measured from the centre of the end pixel to the device physical edge. Saw cuts at distances of 18, 19, 21, 24, 25 and 26 um were made. Except for one particular case, the spurious signal measured after cutting was always less than that measured on a whole wafer. A typical set of measurements is shown in Table I, where the particular case is shown circled. Figure 12 shows typical results.

Three general conclusions may be drawn from the measured data:

(1) The spurious charge in the first and last pixels of the redesigned HSA device is always less than for the standard HSC device. This is attribued to the collection by the guard ring of some of the charge generated beyond the sensor electrodes.

(2) The amount of spurious charge in pixels #2047 and 2048 is always greater than for pixels #2 and 1, respectively. This is because there is more unshielded area near the output than the input.

TABLE I: Percentage increase in measured signal at the input and output edges before and after cutting for HSA, HSC device. [B, A refer to Before and After cutting].

CHIP #	DEVICE TYPE	SAW-CUT DIST FROM CENTRE OF		PERCENTAGE INCREASE IN MEASURED SIGNAL							
				INPUT EDGE				OUTPUT EDGE			
		INPUT PIXEL	OUTPUT PIXEL	PIXEL #1		PIXEL #2		PIXEL #2047		PIXEL #2048	
				B	A	B	A	B	A	B	A
G3	HSA	25	26	35	15	10	0	18	5	59	40
G3	HSC	25	26	50	26	10	0	18	10	100	90
F2	HSA	19	24	22	26	10	0	18	5	50	40
F2	HSC	19	24	31	29	10	0	18	10	106	105

(3) After saw-cutting, the spurious charge tends to decrease. It is believed that the saw-cut damage acts as a sink for charge or, equivalently, reduces the minority carrier lifetime in the immediate region.

5.9 Output Tap Gain (W66A-HSB)

The output signals from the mid-output and end-output taps on the redesigned version were measured and are shown in Figure 13a and b. A small difference in signal level is noticeable, with the output at the end-tap being 5% higher. The reason for this difference in gain is not known as yet, but may be explained by a difference in the total stray capacitance connected to the sensing diffusion or by a charge "print-through" effect.

5.10 Effect of Compensation Implant and Anneal

The compensation implant was matrixed (Figure 5) to determine the resulting effect on saturation and dark current. Increasing the implant dose underneath the Poly 2 electrode essentially increases the bucket height hence increasing saturation. Additional implantation also results in increased crystalline damage and hence an additional contribution to the

general dark current. A special anneal cycle was performed on two wafers (Figure 5) to check whether it would help reduce the dark signal. The number of wafers used for this evalution is too small to obtain any statistical information. However, measurements indicate that a high implant dose followed by an adequate anneal (not necessarily the one used in this matrix) results in a high saturation voltage without additional dark current.

Table II shows the results of preliminary testing on a small number of die. Exhaustive testing for dark current measurements has not been done and results only indicate typical values on a good wafer.

TABLE II: Saturation voltage and dark current levels for different compensation Implant doses. E1 dark current is measured at a master clock frequency of 26 KHz and 28°C; E96 dark current is measured at 260 KHz

Heat Treatment	Compensation Implant Dose	Saturation Voltage		Dark Current, Equivalent Imager Output Voltage	
		E1	E96	E1	E96
	$\#/cm^{-2}$	mV	mV	mV	mV
Not Annealed	1.1×10^{12}	800	490	75	200
Annealed	1.4×10^{12}	1500	625	25	50
Not Annealed	1.4×10^{12}	1200	610	85	160
Not Annealed	1.7×10^{12}	1700	800	120	300

5.11 W66A Device Yield

A total of 78 chips, each containing one HSA, HSB and HSC device are defined on each 100 mm wafer. To obtain an indication of the typical yield that is possible, five wafers were given a 100% device screen test.

Devices were tested electro-optically. A few of the devices that passed this test may be rejected because of a greater number of dark spikes than acceptable by ITEK Standards or because of signal non-uniformity; the latter was not considered because of the absence of a Metal 3. Table III shows the number of good devices that passed the functionality testing. The yield results verify that all redesigned features were correctly implemented.

5.12 Device Operating Voltages

An optimum set of operating voltages for devices W66-HSA, -HSB and -HSC is given in Table IV. These voltage levels are to be used with the prototype devices to be delivered to ITEK. The minimum and maximum usable values for some of the parameters varies greatly. The values shown here have been selected so that only one single change is necessary (the reset voltage) to test all devices.

TABLE III: Number of functional devices per wafer.
Maximum Yield =78

WAFER IDENTIFICATION	DEVICE TYPE		
	HSA	HSB	HSC
JE08A-3	72	65	68
JE08A-4	51	52	54
JE08A-5	65	69	64
JE08A-7	52	56	53
JE08A-9	65	69	64

TABLE IV: Optimum operating voltages for W66A-HSA, -HSB, and -HSC device. (All units are in volts).

Note: All voltages not shown are same as for the E57B imagers.

	DEVICE W66A-			
SYMBOL	HSA	HSB	HSC	COMMENTS
V_{BB},	-5	-5	-5	$\emptyset_{ISR2}$ = -5 volts for HSB, HSC
V_{DD},	20	20	20	V_{DD} must be increased if $\emptyset_R$ is increased
$\emptyset_R$	25	15	25	system limit = 25V. $\emptyset_R$ can be 10V for HSB.
$\emptyset_{C1}$	18	18	18	Min values for A, B, C, are 10, 8, 12 respectively.
$\emptyset_{C2}$	18	18	18	" " " "
$\emptyset_O$	12	12	12	Mid-tap voltage > 8V
$\emptyset_{SS2}$	12	12	12	
$\emptyset_{SS1}$	11	11	11	Min and Max values have
$\emptyset_{SPI}$	11	11	11	a very wide range
$\emptyset_1$-$\emptyset_8$	11	11	11	
V_{DISR}	20	20	20	
V_{DI}	20	20	20	

6. GETTERING CHARACTERIZATION RESULTS, E42C (TASK 2A)

6.1 Introduction

The initial year's work on the E42C CCD Yield Enhancement Test Chip was funded by a BNR Internal R/D capability case. The purpose was to provide suitable device structures for evaluation of

(i) Electro-optical CCD performance,

(ii) Diagnostic information of BCCD (Buried Channel CCD) structures,

(iii) Basic BCCD circuit simulation and verification,

(vi) Statistical information of electro-optical parameter distribution,

(v) BCCD process yield enhancement information especially wrt dark current.

The specific work performed under the BNR case included the design of the test-chip,* photomask procurement, process simulation and experimental design, fabrication of four batches and testing of standard test inserts and some device structures. The matrix of experimental variations was so large (28) that additional funding was required to complete testing of devices relevant to ITEK imager processing. Specifically, the objective of DARPA Contract # MDA 903-81-C-0390, Task 2A was to determine the effectiveness of a variety of process options on the reduction of dark current in silicon imagers.

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*The mask design layout and the device testing procedures are described in reference 5.

6.2 Wafer Fabrication

Four separate batches, a total of 66 wafers, were fabricated with the BNR, 100 mm buried channel NMOS CCD process. A few process steps were matrixed in each batch to investigate particular features relating to imager improvements. The intent of each batch may be briefly stated as follows:

Batch 1: To evaluate three different (one standard, two non-standard) segregation anneal cycle temperatures for the getter cycle at the end of the standard process.

Batch 2: To evaluate different values of the buried channel junction depth and the compensation implant dose.

Batch 3: To investigate the effect of different starting substrates (different manufacturers) on CCD imager performance with and without the addition of a non-standard back-phosphorus implant at the front-end of the process.

Batch 4: To evaluate the effect of non-standard gettering cycles at the front end of the standard process.

6.3 Test Procedures

Testing of this task involved measurements of imager dark current and substrate minority carrier lifetime. The dark current was measured on forty imagers per wafer at a chuck temperature of 27°-30°C and various S/R integration times ranging between 0.82 - 1.64 seconds. [Note: One wafer contains 200 die]. C-V/C-t measurements, at 1 MHz test frequency, were performed on the same die used for measuring dark current to calculate the minority carrier lifetime. A CSM semi-automatic system was used for the capacitance measurements on a Poly 1 capacitor with an area of 10^5 square microns.

6.4 Results

Pertinent results are summarized in Tables V, VI and VII for Batches 1, 3, and 4, respectively. Testing of Batch 2 was not covered by the DARPA Contract and is not presented here. Each of the batches contains a set of wafers processed in the standard way and the results thereof are meant to be used as the "reference standard" for each particular batch. Results in one batch can be compared to the batch reference and to each other but great caution must be exercised in comparing inter-batch results. Although all results in an individual batch may be normalized to the reference standard and then the normalized inter-batch values compared, it is felt that the conclusions derived thereof may still be erroneous. For this reason no single definite conclusion is derived, rather general conclusions will be made.

The results in Table V show that a standard phosphorus backside getter treatment followed by a 1 hr. segregation anneal at 800°C provides the lowest values of dark current and the highest values of minority carrier lifetime when compared to a 1 hr. segregation anneal at 700°C or 600°C. Moreover, 70% of the devices measured had dark currents less than 1 nA/cm^2 and the spread between the maximum and minimum values of dark current was 0.6 nA/cm^2 for a chuck temperature of 29 $\pm$ 1°C. The 800°C segregation anneal is the standard process step used for the E57B getter cycle.

There is some conflicting evidence as to whether a heavy phosphorus implant (1×10^{16} ions/cm^2 @ 200 KeV) at the front end of the process before the subnitride oxidation is beneficial. Table VI shows that the non-gettered Wacker and the gettered Texas Instruments, SEH and SMIEL substrates have lower values of minimum dark current. For the SEH and SMIEL wafers, these values are extremely low, 0.3 nA/cm^2 at 29°C. Although the float zone (SEH) wafers, indicate a high minority carrier lifetime this may be solely due to the higher resistivity of the substrate, since the imager dark current in these wafers was too large for any practical value. The SEH substrates are the standard wafers used for the E57B imagers.

During processing of Batch 4, many problems were encountered including front surface scratch damage during the wafer back implantation. Hence the results obtained from this batch, shown in Table VII, cannot be compared to other batches directly. In fact, the wafers processed in a standard way in this batch have higher dark currents and lower lifetimes than for similar wafers in Batch 1 (Table V). Nevertheless, the wafers that got a back phosphorus implant and/or a phosphorus diffusion have both higher lifetimes and a lower spread of dark current ($I_{dmax} - I_{dmin}$).
Furthermore die on these wafers have dark currents less than 2 nA/cm^2 as compared to the standard wafers, 43% of which have $I_d > 2$ nA/cm^2. Only the minimum and maximum values of the minority carrier lifetime have been presented since the spread between these values is very small. A back implant and diffusion appears to be beneficial to general dark current reduction.

TABLE V: Dark current, I_d, and minority carrier life time, τ, results for different segregation anneal temperatures. Anneal time is 1 hour in all cases.
[T = 29°C ± 1°C; Integration time (S/R) = 0.82 s.]
Note: All wafers get a standard getter cycle at 1050°C.

Anneal Temp.	Dark Current, Id			Lifetime, τ		
	Minimum	Typical	Maximum	Maximum	Typical	Minimum
T°C	nA/cm^2			μS		
800 (Standard)	0.7	0.9	1.3	512	400	216
700	0.9	2.2	2.8	172	150	92
600	1.5	2.5	3.7	95	90	50

TABLE VI: Dark Current, I_d, and minority carrier lifetime, τ, results for different starting materials with (a) standard getter and segregation anneal, (b) standard getter and segregation anneal + a non-standard extra getter cycle at front end of process (back implant = 10^{16} p+/cm^2 @ 200 kEv).

Note: Standard imager substrates are shown circled.

Starting Material		Resistivity	Dark current, I_d, nA/cm^2			Temp. ±0.5	S/R Integration	Min. Carrier Lifetime, τ, uS		
		ohm-cm	Min.	Typical	Max.	Deg. C	Time, S.	Min.	Typical	Max.
CZ Wacker	a	6-10	0.5	0.9	1.1	27	1.64	350	480	620
	b		0.9	1.3	1.5	28.5	1.64	350	480	495
CZ T.I.	a	6-10	1.8	2.4	3.2	28.0	0.82	100	110	115
	b		1.6	1.9	2.6	28.0	1.64	95	120	125
CZ SEH (STANDARD)	a	(6-10)	1.3	1.6	2.1	28.0	1.64	95	160	150
	b		0.3	1.2	2.2	29.5	1.64	215	250	280
CZ SMIEL	a	6-10	0.8	1.4	2.0	28.0	0.84	140	190	215
	b		0.3*	0.6	1.3	28.5	1.64	445	500	615
FZ SEH	a	50-70	-	-	-	-	-	350	470	600
	b		-	-	-	-	-	470	620	750

*Actual numerical values calculated were 0.24 and 0.27 nA/cm^2 at different integration times

TABLE VII: Imager dark current, I_d, and minority carrier lifetime, τ, variations for additional process steps to the front-end of the standard process. All additional steps were performed prior to the sub-nitride oxidation.
[Dark Current is measured at T = 29°C for S/R integration times 1.0 - 1.6 sec. Silicon Substrates, 6-10 ohm-cm, <100>, p-type, SEH].

Additional Process Steps	Dark Current I_d, nA/cm2		% of device with I_d		Minority Carrier lifetime, τ, uS	
	Min.	Max.	<1.5	>2.0	Min.	Max.
NONE: STANDARD PROCESS	0.9	2.5	40	43	140	200
Phosphorus Implant	1.5	2.6	8	73	110	155
Phosphorus Implant + Diffusion	1.2	1.9	30	0	250	305
Phosphorus Diffusion	1.4	2.0	29	0	155	235
Pre-Oxidation Getter	2.3	-	-	100	135	185

7. DUAL DIELECTRIC CCD IMAGERS (TASK 2C - PART 1)

7.1 Introduction

The aim of this part of the DARPA Contract was to evaluate the feasibility of a composite dielectric CCD imager. The composite dielectric used here is a silicon nitride-on-silicon dioxide layer.

The specific work performed may be summarized as follows:

1. Modelling of the thermal cycle for the silicon dioxide layer and the compensation implant energy and dose.

2. Establish the dual dielectric technology and process sequence (Batch JE03A).

3. Evaluate the feasibility of dual dielectric TDI imagers (Batch JE07B).

4. Device testing.

5. Delivery of packaged devices.

This work has been successfully completed. Packaged functional devices have been delivered to ITEK as per contractual obligations.

7.2 Process Modelling

The Stanford University Process Model, SUPREM, was used to model the 700 angstrom gate oxide (SiO_2) thermal cycle at 1000°C in a 2% HCl ambient with user-supplied parameters for the HCl growth rates. The model was also used to select a compensation implant energy and dose in the dual dielectric region such that the final implant profile was similar to the one in the standard process.

7.3 Wafer Fabrication

7.3-1 Fabrication of Batch JE03A

Test batch JE03A was fabricated to establish the dual dielectric technology and the process sequence applicable for implementation of such technology in the standard buried channel CCD process. Starting material for this batch of 10 wafers was 100 mm, 6-10 ohm-cm, CZ, <100>, silicon.

The 700 Å SiO_2 gate thermal cycle, as modelled in Section 7.1, was verified to be correct as was the particular compensation implant and dose. The 400 Å thick nitride layer was deposited by a low pressure CVD technique. Thickness and uniformity measurements were made on the IBM 7840 Film Thickness Analyzer. The thickness measurements were cross-checked on the NanoSpec Automatic Film Thickness System and the Tencor Alpha-Step surface profilometer. The oxide thickness measured over some 200 locations on the wafer was 700 $\pm$ 30 Å and the nitride layer was 400 $\pm$ 40 Å. Figures 14 and 15 show typical uniformity measurements for these layers.

Etching experiments showed that both plasma and wet etching may be used for the selective removal of the densified nitride. For the time required to delineate the nitride, the plasma etching process removes less than 200 Å of polysilicon. Wet etching of the nitride does not appear to remove any polysilicon.

7.3-2 Fabrication of Batch JE07B

Batch JE07B was fabricated to evaluate the feasibility of dual dielectric TDI CCD imagers. Using the technology derived from Section 7.2-1 a few steps of the standard BCCD process were substituted with alternate steps to allow for the incorporation of a dual dielectric gate. A large part (>80%) of the standard process was left untouched. 17 wafers were processed in all. Wafers #1-12 were processed with a dual dielectric while wafers 13-17, the reference arm of the matrix, were fabricated with the standard BCCD

process for comparison purposes. All steps common to both processes were fabricated simultaneously. This batch was susceptible to the same fabrication problems as its companion batch, JE07A, discussed in Section 4, except for the intermetal dielectric deposition steps.

The W62A TDI test mask[6] was used for evaluation of the dual dielectric process. The mask consists of a 96 x 512 element TDI imager.

7.4 Test Results of Dual Dielectric TDI Imagers

The imagers were tested in the manner described in reference 6. The die yield on all wafers was typically 57%. All devices, including those with standard processing, had average dark current levels of 7.8 nA/cm^2 at a temperature of 29°C. This value of dark current is approximately five times larger than what is normally observed. These high dark current levels are thought to be related to processing problems at the time of fabrication. Table VIII shows some results obtained on these imagers. The relative sensitivity appears to be slightly higher for the dual dielectric imagers. This value is measured under uniform light conditions for a set reference light level and a master clock frequency of 260 KHz. The MTF for these devices is excellent and the S/R transfer efficiency is better than 0.99997. Figure 16 shows typical outputs at 1 MHz and 260 KHz master clock frequencies for 50 mV signal levels. Figures 16a and b show typical outputs for a focussed test bar pattern. The variation in the output signal non-uniformity is caused by defects in the test pattern and associated projector light. Figures 17a and b show the shift register output for a series of 16 "ones" followed by a long string of "zeroes" obtained by a fill-and-spill diode input technique. An expanded version of these outputs is shown in Figures 17c and d. The split video (approx. 10%) at the end tap is visible in the latter figures. Charge print-through ($\lesssim$10%), due to incomplete destructive signal readout at the mid-tap, has been observed on some die.

TABLE VIII: TDI Imager Test Results

DESCRIPTION	DUAL DIELECTRIC TDI IMAGERS			STANDARD BCCD TDI IMAGERS			COMMENTS
	MIN.	AVERAGE	MAX.	MIN.	AVERAGE	MAX.	
El Saturation, V	1.5	1.6	1.8	1.1	1.2	1.5	-
Dark Current, nA/cm^2	4.1	7.1	9.5	6.8	8.5	11.1	Temp = 29°C $\pm$ 1°C
Relative Sensitivity, mV	220	240	300	175	190	220	Lamp Voltage set at 850 mV. Freq. = 260 KHz
S/R Transfer Efficiency	-	> 0.99997	-	-	> 0.99997	-	Freq. = 260 KHz

7.5 Device Assembly and Deliverables

Two wafers (#3 and #7) were diced up from which functional devices were sorted and assembled in 40-pin dual-in-line packages. Figure 18 shows the description of the device bonding pad while Figure 19 shows the bonding diagram. The devices were sealed with quartz lids and branded. The brand names used, DD3-PR and DD7-SX are for internal reference only. The pin-number, mnemonics and functional description for these devices are given in Table IX. The voltage levels for optimum operation of these devices are given in Table X.

TABLE IX:

DD3-PR and DD7-SX Package Pin No., Mnemonic and Functional Description

Pin No.	Mnemonic	Description
1	Ø8L	Lower eight phase ripple clock electrode
2	ØI2	Electrical input control gate of TDI sensors (Poly 2)
3	ØI1	Electrical input control gate ot TDI sensors (Poly 1)
4	Ø7L	Lower eight phase ripple clock electrode
5	Ø6L	" "
6	Ø5L	" "
7	Ø4L	" "
8	Ø3L	" "
9	Ø2L	" "
10	DI	Input diode diffusion for TDI
11	GNDS	Scribe channel
12	Ø8U	Upper eight phase ripple clock electrode
13	Ø7U	" "
14	Ø6U	" "
15	Ø5U	" "
16	Ø4U	" "
17	Ø3U	" "
18	Ø2U	" "
19	GNDU	Upper guard ring and light shield
20	Ø1U	Upper eight phase ripple clock electrode
21	N/C	No connection
22	DISR	Input diode diffusion of serial shift register
23	N/C	No connection
24	ØISR2	Input control/gate of serial shift register (Poly 2)

TABLE IX (cont'd)

Pin No.	Mnemonic	Description
25	ØISR1	Input control/gate of serial shift register (Poly 1)
26	ØC2	Clock electrode of 2 phase serial shift register (Phase 2; It connects all even electrodes)
27	Ø1L	Lower eight phase ripple clock electrode closest to the shift register
28	ØSSI	Poly 2 transfer electrode between 1st row of sensors and the storage electrode SPI
29	ØSPI	Poly 1 storage electrode for the serial to parallel transfer operation
30	ØSS2	Poly 2 transfer electrode between SPI and the serial shift register
31	ØC1	Clock electrode of 2 phase serial shift register. (Phase 1: It connects all odd electrodes)
32	V_{BB}	Substrate
33	O/PM	Mid-tap video output
34	ØOM	Enable gate of the mid output circuit
35	ØOE	Enable gate of the end output circuit
36	ØR	Reset gate
37	V_{DD}	Drain voltage connection for both the mid and end output circuits
38	GNDL	Lower guard band and light shield
39	O/PE	End video output
40	N/C	No connection

TABLE X: Voltage levels for DD3-PR, DD7-SX

ELECTRODES		OPTIMUM	MIN.	MAX.
$\phi_{2L} - \phi_{8L}$		11 V DC (ripple clock, E96)	2	15
ϕ_{1L}	E96	" " "	"	"
	E1	0	0	0
$\phi_{1U} - \phi_{8U}$		11 V DC (ripple clock, E96)	2	15
DI		VDD	V_{DD}	V_{DD}
ϕ_{I1} (POLY 1)	E1	12	$\phi_{2L}-\phi_{1L}+2$	15
	E96	0	0	0
ϕ_{I2} (POLY 2)	E1	12	$\phi_{2L}-\phi_{1L}+2$	15
	E96	0	0	0
GNDS		0	0	0
GNDU		0	0	10
GNDL		0	0	10
DISR		V_{DD}	V_{DD}	V_{DD}
ϕ_{ISR2} (POLY 2)		0	0	0
ϕ_{ISR1} (POLY 1)		ϕ_{C1} clock	-	-
ϕ_{C2}		18 V (22)	11	22
ϕ_{C1}		18 V (22)	11	22
ϕ_{SS1}		0 - 11 V (+VE PULSE)	2	15
ϕ_{SPI}		11 - 2 V (-VE PULSE)	2	15
ϕ_{SS2}		0 - 12 V (+VE PULSE)	2	15
V_{BB}		-5 V (-3)	0	-13
ϕ_{OM}, ϕ_{OE}		10 V	8	16
ϕ_R		25 V	24	26
V_{DD}		20 V (18)	14	21

8. HIPOX CCD IMAGERS (TASK 2B & TASK 2C - PART 2)

8.1 Introduction

This sub-task investigated the feasibility of using high pressure oxidation (HIPOX) techniques as a viable alternative to standard (atmospheric pressure) oxidation techniques in our buried channel CCD process. If viable, the advantages of growing "good" thermal oxides at significantly lower temperatures and reduced processing time are self evident.

The specific work performed may be summarized as follows:

(1) Modelling of high pressure oxidation and anneal cycles. Subsitution of the new HIPOX cycles in the standard buried channel process and optimization of the altered process.

(2) Wafer fabrication of Batch JE08B (25 wafers) using the W62 test mask to evaluate the feasibility of the HIPOX process.

(3) Testing of the imager devices and test inserts.

(4) Delivery of packaged devices to meet contractual commitments.

A parallel research program on high pressure oxidation, funded internally, provided modelling parameters and all necessary process techniques.

This task has now been successfully completed. Packaged functional devices have been delivered to ITEK as per contractual obligations.

8.2 Process Modelling

The process model, SUPREM, was used to model the field oxide and the gate oxide thermal cycles with user-supplied parameters available from the internal capability work and reported in references [7] and [8]. The high

pressure process was modelled for various cycle temperatures between 900°C and 1050°C. The optimum cycle was dictated by the need to minimize the sideways diffusion of the field threshold (V_{TIF}) implant. The optimum field oxide cycle temperature was 920°C at 10 atmospheres pressure. The field threshold implant had to be remodelled and optimized so that the parametric values of the standard process were maintained or improved. With the available data, it was found necessary to double the V_{TIF} implant energy to compensate for the fast high pressure oxide growth and the relatively slow diffusion of the V_{TIF} boron implant at 920°C. Various other anneal cycles, both at high and low pressure, were modelled and subsequently incorporated into the complete process model. These anneal cycles were deemed necessary as compensation for the lower general temperatures used.

8.3 Wafer Fabrication

Batch JE08B was fabricated to verify the process modelling results and to evaluate the feasibility of using high pressure oxidation for processing CCD imagers. Figure 20 shows the matrixing of the 25 wafers used for this batch. Five of these wafers, #19-23, were processed with the standard CCD process throughout for use as the reference arm of the matrix. Process steps that are standard for all wafers are not shown in Figure 20. Steps common to all wafers were processed simultaneously. A phenomenon, where small sections of the second gate oxide around the wafer periphery appear to have a different coloration than the rest of the oxide, is still under investigation.

The W62A test mask, the same mask that was used to evaluate the dual dielectric imagers (Section 7.2-2) was also used for this batch.

8.4 Test Results

Table XI compares some modelled and measured parameters. Both values are in good agreement. The variation in the threshold voltage values for Wafers

TABLE XI: Modelled and measured parameter values for Batch JE08B

PARAMETER		MODELLED VALUE	MEASURED VALUE	COMMENTS
Field Oxide Thickness, um	High Pressure Standard	1.3 ± 0.05 1.2 ± 0.05	1.27 1.16	920° ± 2°; 10 ± 0.2 atm 1000°C ± 1°C; 1 atm
Intermediate Field Threshold Voltage, Volts	High Pressure Standard	25 22	25.5 25.5	
Field Implant Sideways Diffusion, um	High Pressure Standard	0.9 1.2	- -	
Gate Oxide Thickness, Angstroms POLY 1 (POLY 2)	STD. High Pressure High Pressure	1065 ± 30 1000 ± 50 1100 ± 50	1075 (1031) 1041 (1037) 1089 (1100)	WAF #1-5, 19-23: 1050° ± 1°C WAF #9-18; 920° ± 2°C; 10 ± 0.2 atm WAF #6-8. Including a high pressure anneal
Average Threshold Voltage, (Poly 1 Enhancement), Volts	Waf #1-5, 19-23 Waf #9-18 Waf #6-8	0.55 ± .05 0.55 ± .05 0.60 ± .05	0.54 0.54 0.59	# of measurements; Variance; Std. Dev. 59 .0002 .013 60 .0009 .030 18 .0002 .015

#9-18 is much greater than for the other Poly 1 gates as evidenced by the standard deviation values shown. The reason for this is not yet known. In general, all other device parameters were as expected.

The imagers were tested as described in reference [6]. The yield was very high. Two wafers that were 100% tested showed a yield of 41% and 51% for excellent devices (fully functional, no dark spikes) and 70% and 85% for functional devices. Shift register transfer efficiency for optimized voltage levels is greater than 0.99995 as shown in Figure 21a. S/R clock voltages used for this device are 4 V higher than the standard clock voltages (18 V) used for the ITEK E57B device. At 18 V, signal tailing (rounding) occurs as shown in Figure 21b. Further testing is required to clarify the reason for the tailing effect and for the increased value of optimum clocked voltages. Table XII summarizes a few parameters for inter-matrix comparison. All wafers with high pressure oxidation cycles have higher dark current values, saturation voltages and relative sensitivity. The latter was measured as described in Section 7.4. Increased values of dark current may be due to the lower processing temperatures and the absence of HCl in the gas ambient during oxidation. The optical MTF is good for all wafers.

8.5 Device Assembly and Deliverables

One wafer, #12, was diced up, functional devices sorted out and assembled in 40-pin dual-in-line packages. This wafer was chosen because it includes both the high pressure field and gate oxidations. Figure 18 describes the device bonding pads while Figure 19 shows the bonding diagram. The packaged devices were sealed with quartz lids and branded. The brand names used are HP12, HP12-HZ. The pin-number, mnemonics and functional description for these devices are given in Table IX. The voltage levels for optimum operation of these devices are basically the same as those shown in Table X for the Dual Dielectric devices. Table XII(a) shows only the parameters that require applied voltages different from those shown in Table X.

TABLE XII: Comparison of parameter values for different branches of process matrix shown in Figure 20.

	Dark Current @ 28.5±0.5°C	E1 SATURATION VOLTAGE	RELATIVE SENSITIVITY
	nA/cm^2	mV	mV
WAF #1-5	4.8	1300	300
WAF #6-8	7.7	1700	220
WAF #9-13	4.9	1900	325
WAF #14-18	6.4	1800	280
WAF #19-23 (STANDARD)	4.1	1500	200

TABLE XII(a): Voltage levels for HP12 and HP12-HZ devices

Note: The voltage levels for parameters not shown here are the same as given in Table X.

ELECTRODES	VOLTAGE LEVELS FOR E1 and E96		
	OPTIMUM	MINIMUM	MAXIMUM
$\emptyset_{C2}$	22	21	26
$\emptyset_{C1}$	22	21	26
V_{BB}	-3	0	-5
$\emptyset_{OM}$, $\emptyset_{OE}$	10	7	18
V_{DD}	19	12	20

9. MATERIAL (ELECTRODE) INVESTIGATION

9.1 Introduction

This sub-task was originally proposed to investigate the properties of amorphous silicon as an electrode material. Low Pressure, Chemical Vapour Deposition (LPCVD) of this material was envisaged as the source of α-Si at that time. Although attempts were made to include α-Si deposited using other techniques, only one other supplier of material responded in time.

Refractory metal silicides and polycides were also investigated for use as low resistivity electrode materials. Since very little is known about the optical properties of these materials, these properties were examined for four refractory metal silicides. Only one deposition technique was investigated.

Specifically, the work done under this sub-task, may be summarized as follows:

(1) Literature Search

(2) Development of Technology for doped and undoped LPCVD amorphous silicon deposited in range 500-600°C.

(3) Measurement and Comparison of spectral response (190-900 Å bandwidth) of doped and undoped α-Si to polysilicon.

(4) Deposition and preliminary characterization of refractory metal silicides and polycides.

The work covered by this sub-task is now completed.

9.2 Literature Search

Although the technical literature describes amorphous silicon deposition and the material properties realized by particular techniques, no information could be found regarding the incorporation of amorphous silicon into a typical process for silicon imagers while retaining the properties of the as-deposited material. The information regarding electrode materials for charge coupled device TDI imagers appears to be mainly restricted to polysilicon electrodes for the visible light bandwidth[9]. No information could be found regarding the possible utilization of refractory metal silicides and polycides for use in our buried channel CCD process.

9.3 LPCVD Amorphous Silicon

LPCVD silicon films deposited at 580°C were shown to be amorphous by Kamins et al[10]. Kamins investigated silicon films deposited between 525 and 725°C. Our initial work in this area

(i) Duplicated the LPCVD α-Si deposition as reported by Kamins.
(ii) Extended the deposition temperature to 500°C.
(iii) Investigated the deposition of in situ doped amorphous silicon.

Results from the initial test runs established the technology of LPCVD α-Si deposition down to 500°C. Deposition rates for various conditions of gas flows, temperatures and pressures as well as the effect of subsequent annealing (900°C in N_2 ambient) on the resulting thickness are reported in reference [11], both for undoped and in situ phosphorus doped amorphous silicon. The deposition rate drops off, as the temperature is lowered from 625°C to 500°C, by a factor of 50 for undoped silicon and by a factor of 10 for phosphorus doped silicon, with both processes showing deposition rates of 4 ± 1 Å /min. at 500°C.

Batch JE08C (16 wafers) was fabricated to verify the above technology. Amorphous silicon was deposited on oxidized silicon wafers at 580°C, 550°C

and 500°C. A standard polysilicon deposition (625°C) was used as reference. The oxide thickness on the substrate was 1.5 μm. Thickness measurements of the silicon using the IBM 7840 (Film Thickness Analyzer) and cross checked by a Nanometrics Nanospec Automatic film thickness apparatus verified the deposition rates. The uniformity of the deposited films was exceptionally good even at the lower temperatures. Measurements show variations of less than 50 Å for a deposition thickness of 3900 Å. Subsequent x-ray diffraction experiments verified that, at 580°C and below, the deposited silicon material was amorphous. The in situ doped material was mostly amorphous at 580°C and completely amorphous at 550°C and below. For the 580°C samples, certain lines appeared on the x-ray pattern and it could not be unambiguously determined whether this was the result of silicon crystallinity or inter-facial interference. Normalized values of V/I = 2.8 ohms were measured for the in situ doped 550°C amorphous silicon after a gate oxidation (1050°C). A comparative value for in situ doped 625°C polysilicon was 5.0 ohms. V/I was measured by a four point probe technique.

Batch JE25A (8 wafers) was fabricated to measure the spectral response of the amorphous material and to compare it to standard polysilicon material. The spectral response was measured by a Beckman, Model DU-8, UV/visible spectrophotometer. A blank quartz wafer is used as a base reading. Polysilicon at 625°C and amorphous silicon at 550°C were deposited on quartz wafers. The undoped and in situ doped layers were 0.37 $\pm$ 0.05 microns thick. Figures 22-25 compare the various samples in the visible/near IR region. Readings in the 850-900 nm region are very erratic. The shift in frequency between the doped and undoped samples is due to the phosphorus content of the doped samples. Doped amorphous and doped polysilicon samples show better spectral uniformity. This is attributed to the slower deposition rates of the doped material which renders it more uniform. Doped samples show a higher spectral response in general, particularly in the lower end of the spectrum. Figure 26 shows the spectral response for the dc glow discharge hydrogenated amorphous silicon samples. This silicon was deposited at 300°C as follows:

Sample 21-5-82, discharge voltage = 700V, discharge current = 0.65 mA; Sample 26-5-82, discharge voltage = 750V, discharge current = 1.1 mA. The spectral response is found to be rather non-uniform over the sample. It is not known whether this is due to equipment limitations or a subtle reality typical of the dc glow discharge deposition technique. Reduction of discharge voltage and current during deposition enhances optical transmission.

9.4 Polycides and Silicides

The term "polycide" refers to a thin silicide layer deposited on top of polysilicon. Batch JE23B was fabricated to perform a preliminary investigation of polycides and silicides. Four different materials, $TaSi_2$, $TiSi_2$, $MoSi_2$ and WSi_2 were deposited at Perkin Elmer facilities, Mountain View, California with the PE4400 system. The silicides were deposited in alternate layers of metal and silicon, each 30-50 angstroms thick, for a total thickness of 3000 Å on pre-cleaned quartz wafers. For polycides, the silicide layer was 750 Å thick and the LPCVD polysilicon layer on the quartz wafer was 3000 Å thick. All depositions were quasi-stoichiometric, approximately 2:1, but always slightly silicon rich (<10% excess silicon).

The silicide samples do not transmit any light either before or after thermal anneal. Their reflection characteristics do not change after annealing. Table XIII compares the various V/I ratios obtained by using a four point probe technique. Annealing was performed in Argon for 1 hour at temperatures of 700°C, 800°C and 900°C. Samples were inserted into the anneal furnace at 550°C and ramp rates of $\pm$8°C per min. Annealing resulted in significant crystallization and pinholes in the material. The reason for this is still being investigated.

The polycide wafers (750 Å silicide + 3000°A polysilicon) were tested and found to be opaque. A sequence of plasma etches was performed to determine etch rates and 250 Å of the silicide was etched from each wafer. The

optical response of these materials was measured and is shown in Figure 27. At 500 Å the material is slightly transparent without reduction of the sheet resistivity. It is believed that thinner polycides may transmit acceptable light levels while maintaining low sheet resistivity.

TABLE XIII: Comparison of V/I ratios for 3000 Å thick silicides deposited on quartz, for various anneal cycles

[Note: After 900 °C, $MoSi_2$ and Ta Si_2 layers had unreasonably large values of V/I]

MATERIAL TYPE	V/I, ohms			
	As-Deposited:	AFTER ANNEALING AT		
		700°C	800 °C	900°C
WSi2	34.5	33	21.4	13.0
MoSi2	10.5	40-200	2.9	-
TiSi2	18.0	5.5	2.7	4.6
TaSi2	27.5	51.0	> 200	-

10. CONCLUSIONS

The design, processing and testing of the W66 TDI test mask verified that all design modifications have been correctly implemented. This information has proven extremely useful and it is believed that most of the design improvements will be incorporated during 1983 into the next version of the large ITEK 96 x 2048 TDI imager.

The gettering characterization results are very encouraging; dark current values as low as 0.3 nA/cm^2 are achievable. The segregation anneal step at 800°C, which is integral to the standard E57B getter cycle, results in low imager dark current values. The correct choice of starting material together with suitable getter cycles is imperative for minimizing dark current. A getter cycle at the front end of the process, such as a phosphorus implant and anneal, together with the standard getter cycle used for the E57B imager produced the lowest values of imager dark current to date. It is not absolutely clear whether additional phosphorus incorporation via a back-diffusion at the front end of the process reduces the minimum value of dark current (0.3 nA/cm^2) that was achieved. However, it does reduce the spread between the minimum and maximum value of dark current.

The dual-dielectric investigation established this technology capability in our standard process. The reliability of the process models were verified. Although fabrication of the test batch occurred when the development laboratory incurred several processing problems, functional testing proved that dual-dielectric TDI imagers are feasible. The high values of optical sensitivity, transfer efficiency and saturation that were observed make dual dielectric technology a candidate for the future imager development. More complete optical testing by ITEK of the packaged devices is now anticipated.

Modelling results of the BCCD imager process using HIPOX cycles were verified. Functional testing of these devices results in a high yield of

high performance imagers. Improved field threshold voltage, reduced sideways diffusion of the field implant and increased values of saturation voltage and optical sensitivity were demonstrated. The use of high pressure oxidation in the buried channel CCD process is feasible and can significantly improve performance. More detailed electro-optical testing of these imagers by ITEK will help evaluate further the benefits of this process technology.

The electrode material information has been very positive. The optical characteristics of LPCVD doped and undoped silicon deposited at temperatures below 600°C were impressively uniform over 100-mm wafers. Thin layers of silicides (500Å) transmit light partially. With the limited information available, it is not immediately apparent whether amorphous silicon, silicides and/or polycides are directly applicable to our CCD structures. More work in this area is needed before a definite decision can be taken.

11. SUGGESTIONS FOR FUTURE WORK

1. W66A mask set update (i) to standardize current designs, (ii) to implement new, advanced designs to achieve high speed operation and on-chip signal processing, (iii) to evaluate process enhancements such as selective lifetime killing techniques.

2. Conduct preliminary design/process evaluation on next generation imager technology.

3. Process development of a practical virtual phase CCD.

4. Fast neutron irradiation for lifetime control.

5. Evaluate α-Si:H for potential application as photoconductor sensor electrodes integrated with CCD structures to form hybrid sensors.

6. Investigation of narrow-band filters compatible with monolithic CCD imagers.

7. Detailed electro-optical characterization and process fabrication of new silicon-based electrode materials.

8. Development of groove technology for channel separation and buttable edge etch protection.

9. Preliminary investigation of back interconnection techniques.

12. ACKNOWLEDGEMENTS

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14. FIGURES

W66A DESIGN

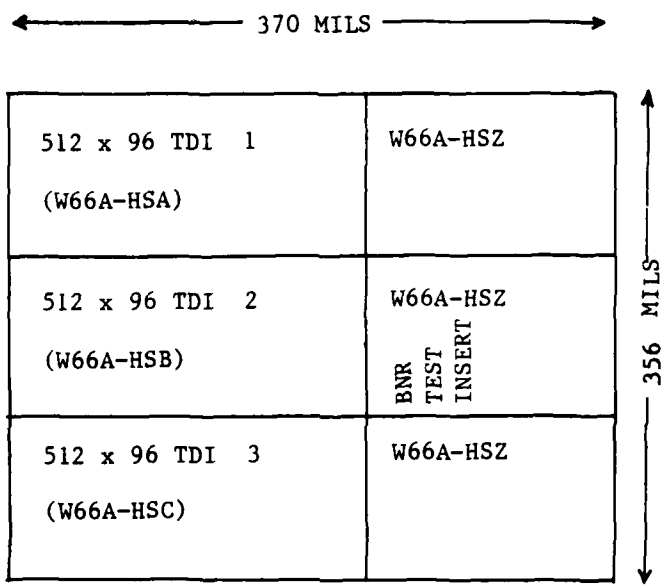


FIGURE 1: Organization of W66A

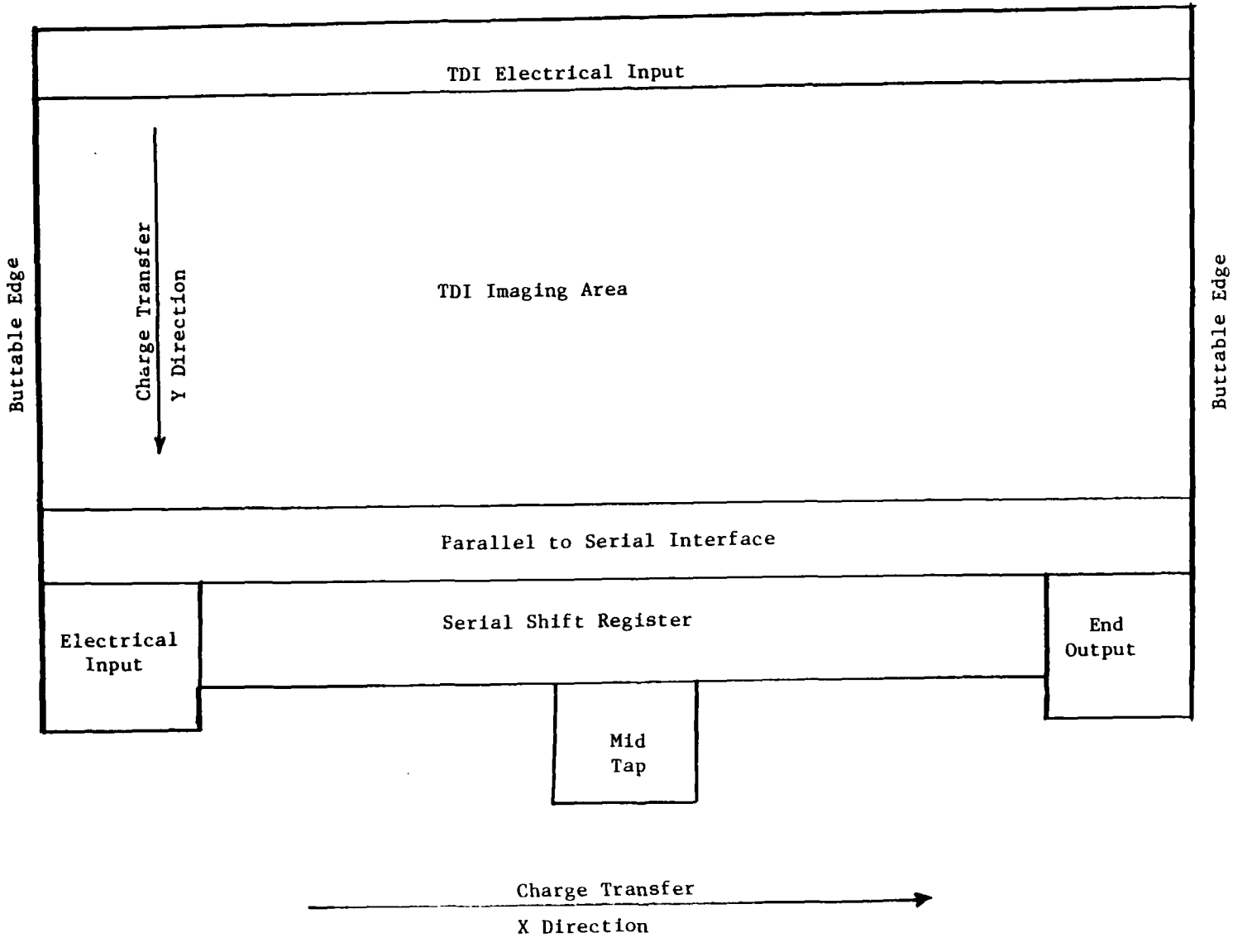
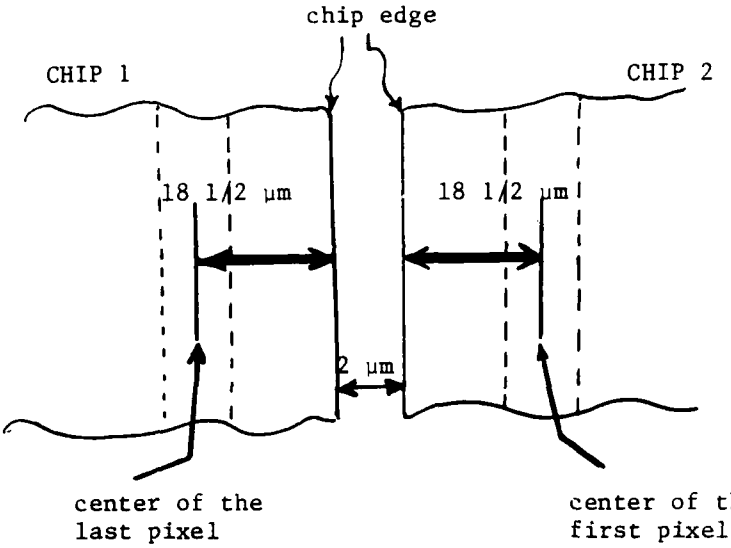


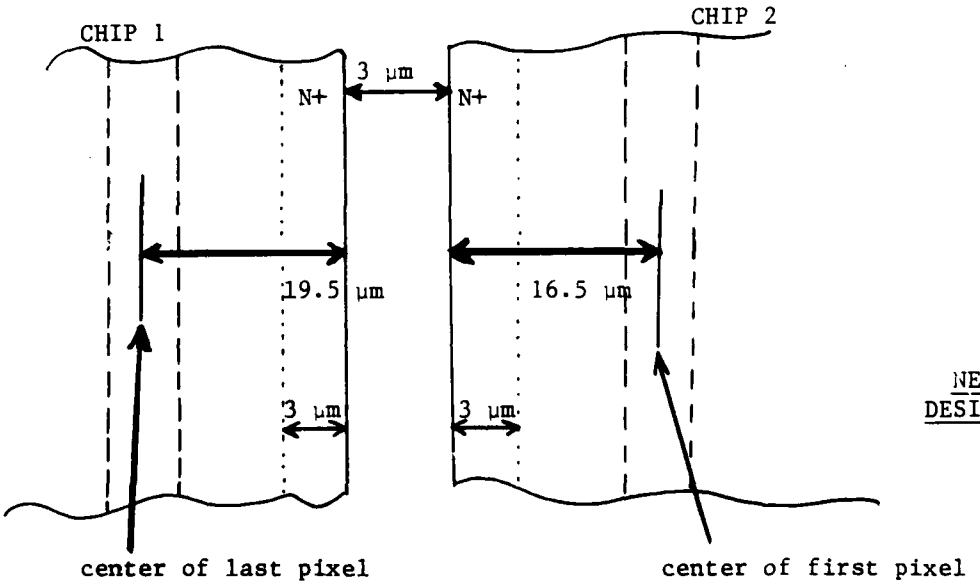
FIGURE 2: Block Diagram of the 512 x 96 Buttable TDI Imager



OLD DESIGN

TOTAL SEPARATION BETWEEN THE CENTER OF LAST PIXEL OF CHIP 1 TO THE CENTER OF FIRST PIXEL OF CHIP 2

= 18 1/2 + 2 + 18 1/2 = 39 µm



NEW DESIGN

CENTER OF LAST PIXEL TO CENTER OF FIRST PIXEL SEPARATION

= 19.5 + 3 + 16.5 = 39 µm

FIGURE 3· Redesign of the buttable edge circuitry

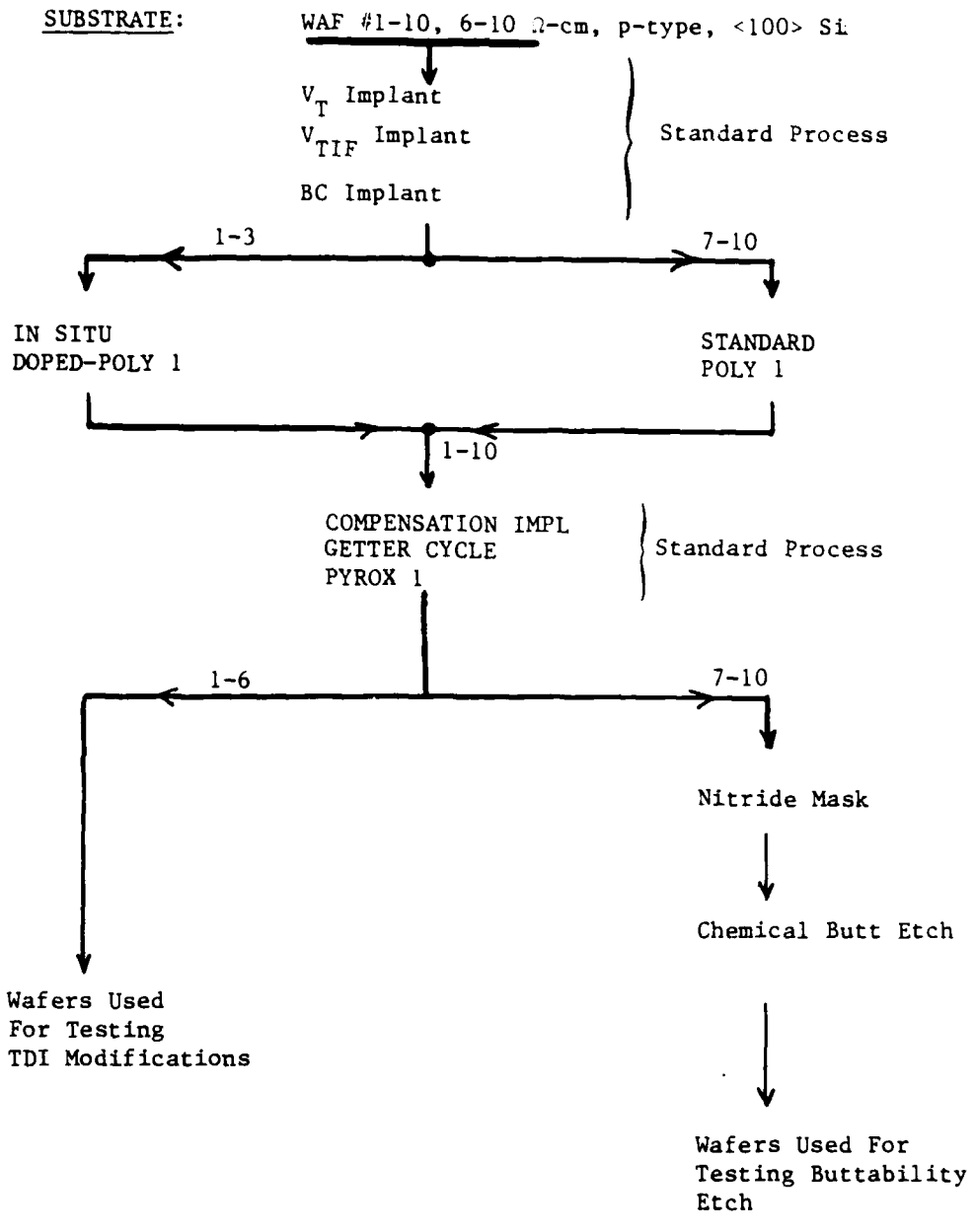


FIGURE 4: Salient features of process matrix for Batch 1 (JE07A)

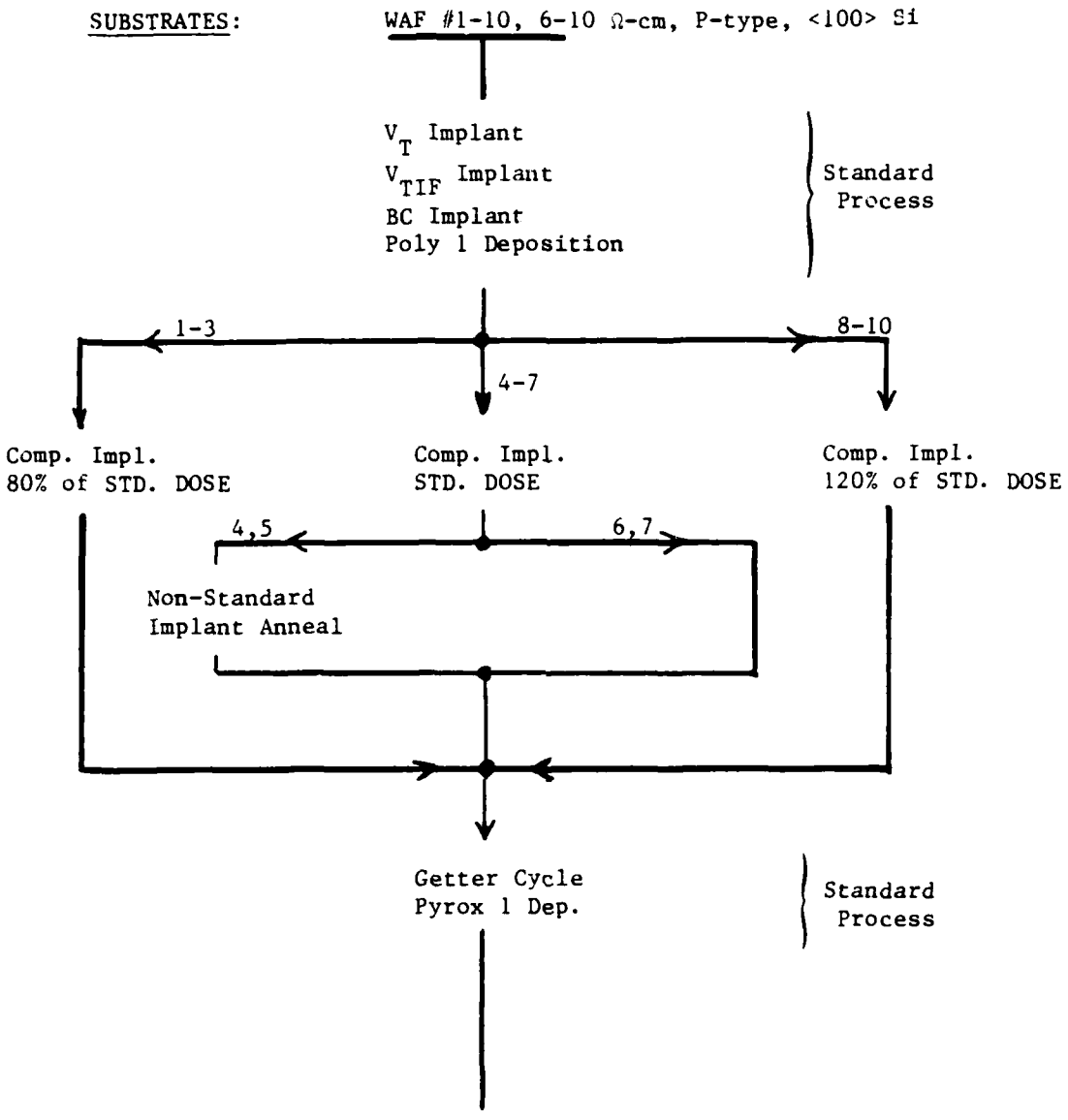
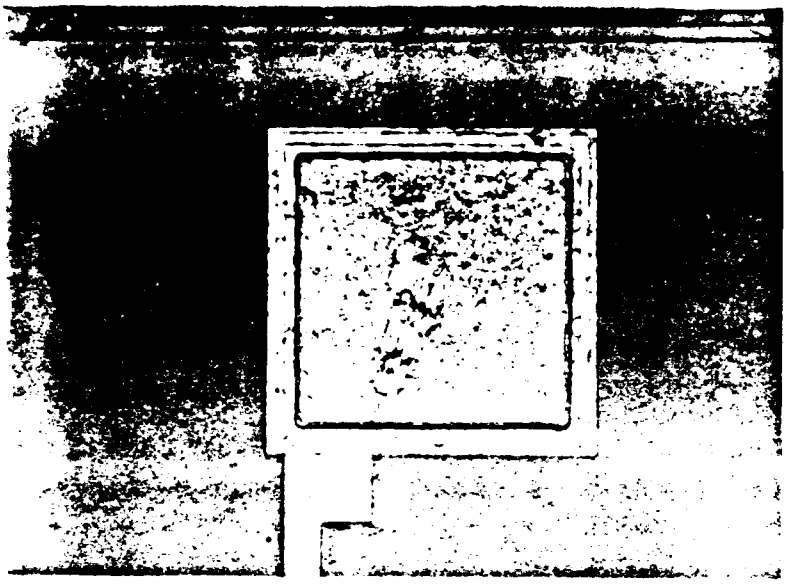


FIGURE 5: Salient features of Process Matrix for Batch 2 (JE08A)

(a)



(b)

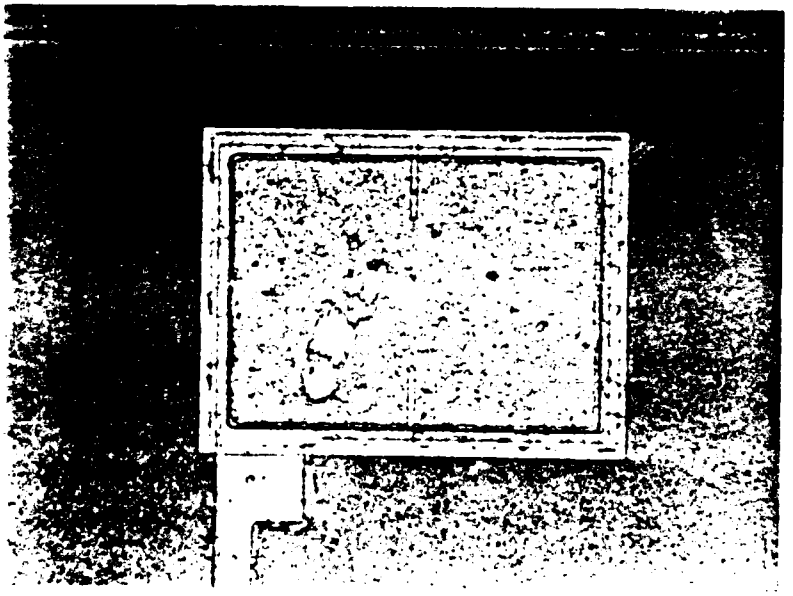
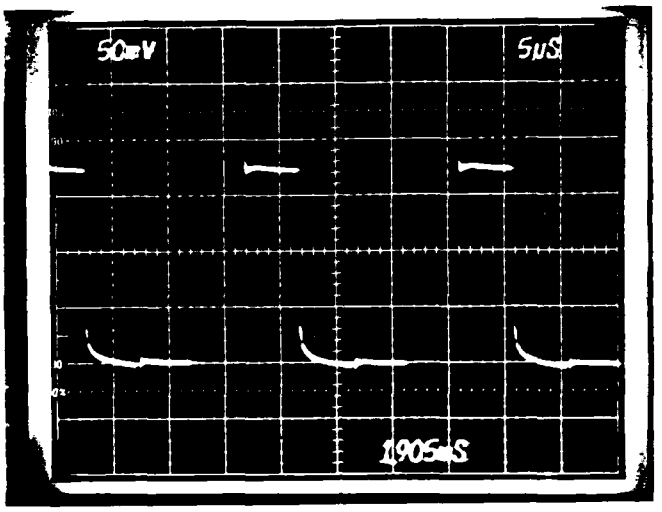


FIGURE 6: Redesign version of the bonding pad
(a) Original pad, 125 microns x 125 microns
(b) Redesigned pad, 140 microns x 250 microns
Note how the probe mark in (b) is retained in the left half of the enlarged pad.

(a)



(b)

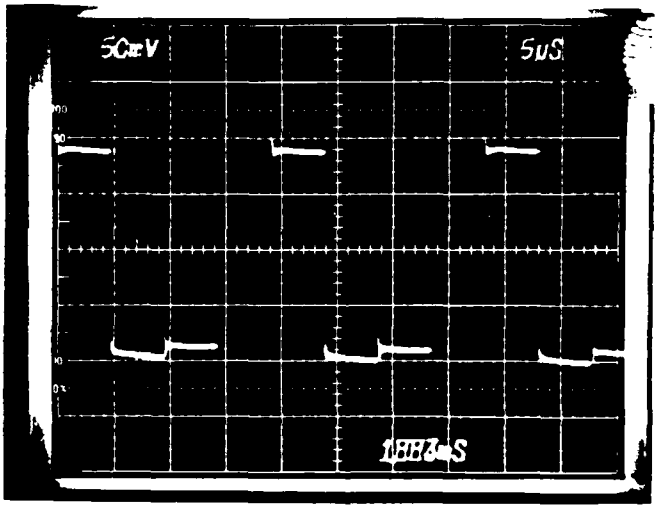


FIGURE 7: E1 output video signal for the W66A-HSA device with $\emptyset_{C1}$ = 18V. (a) mid-output; (b) end-output
This device is tested in wafer form.

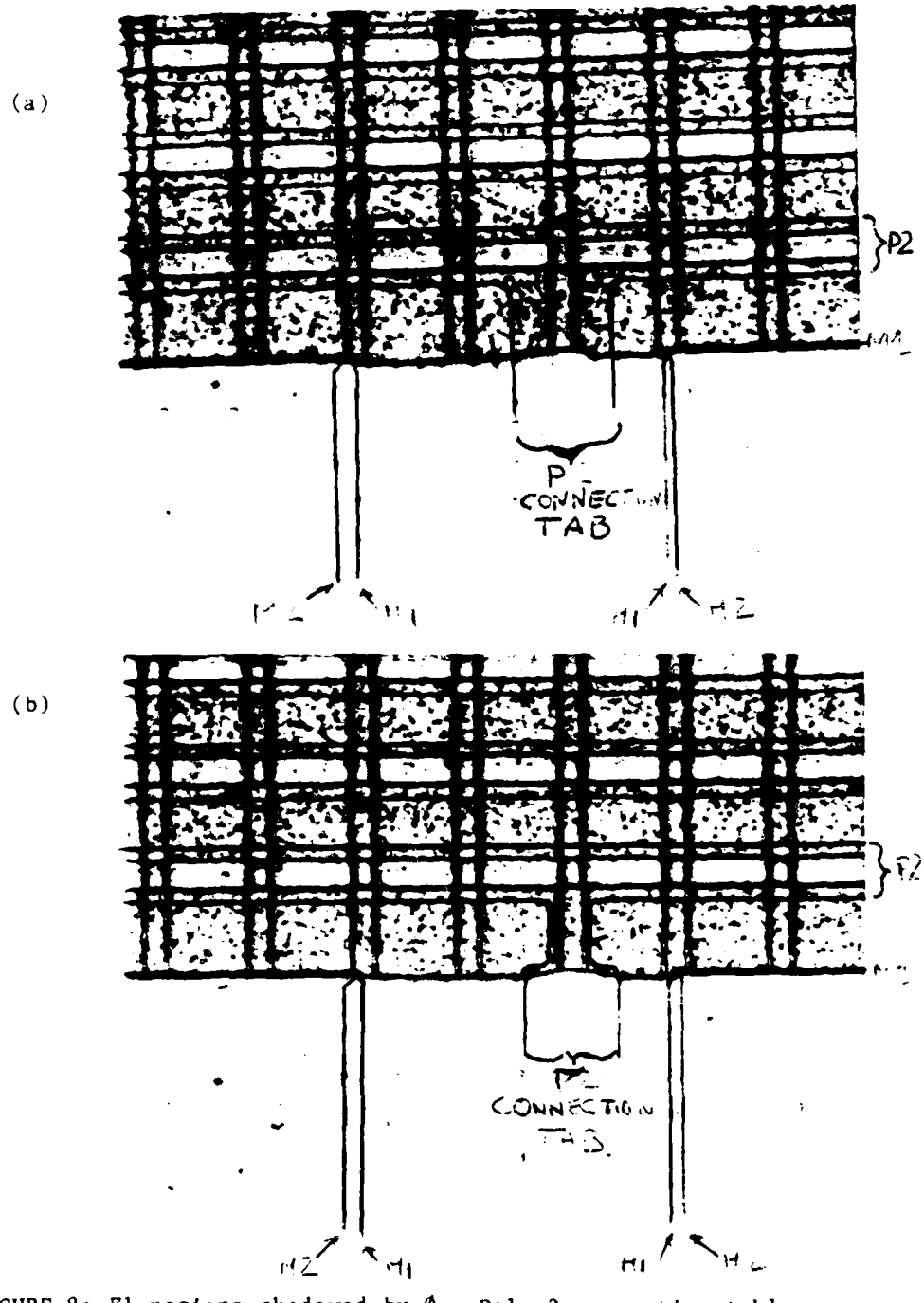


FIGURE 8: El regions shadowed by $\emptyset_{1L}$ Poly 2 connection table.
(a) Original version, device 'C'; (b) redesign version device 'B'.
Also visible is M_2 to M_1 misalignment.

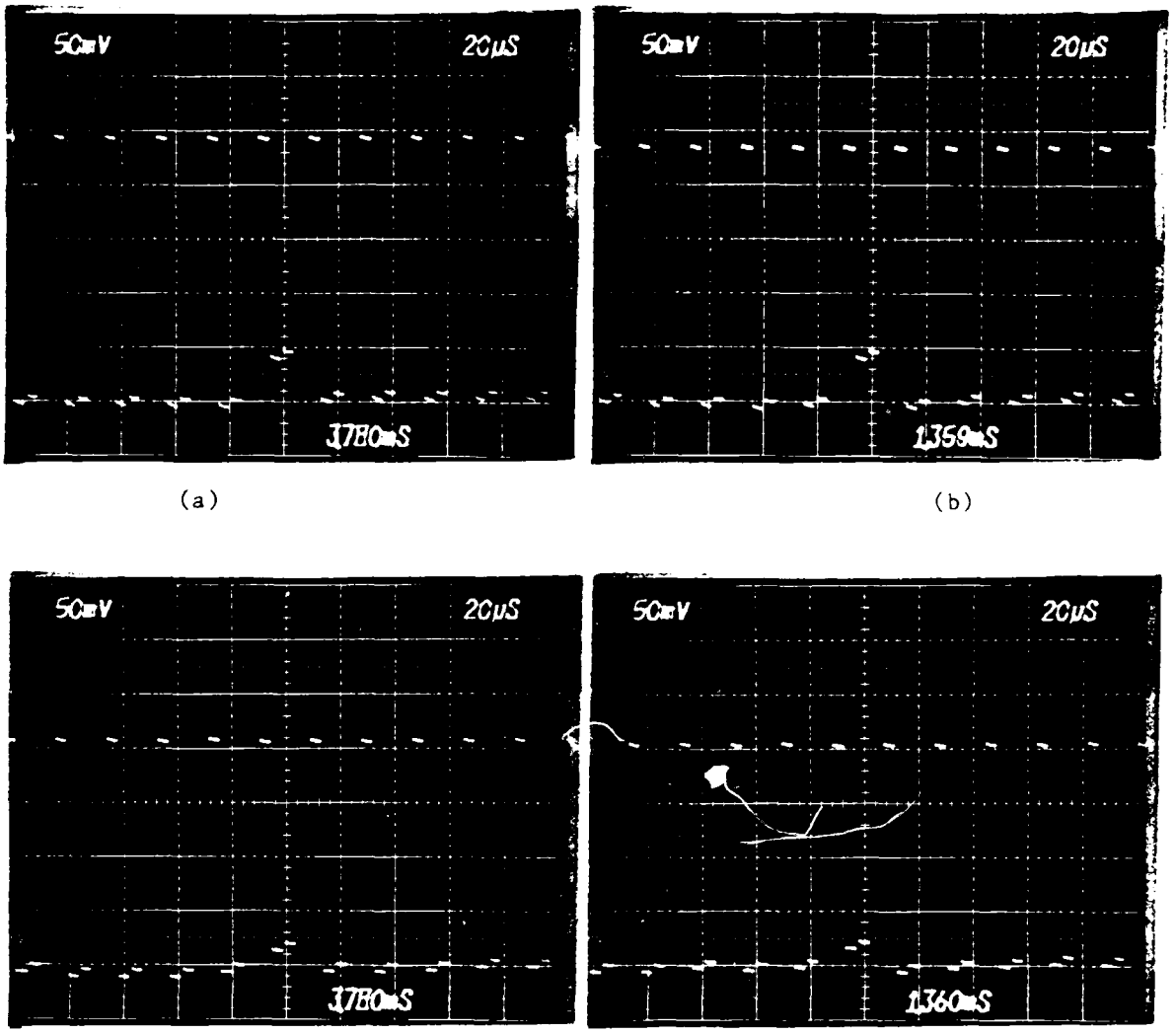
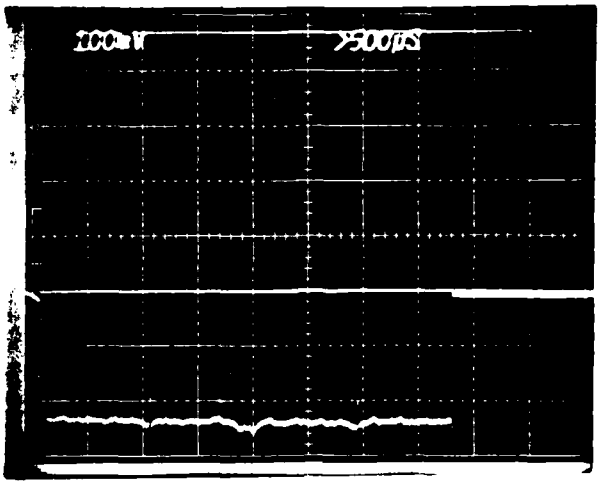
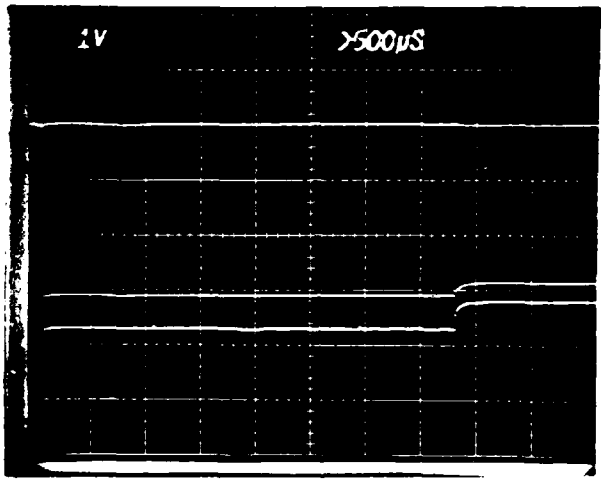


FIGURE 9: Video signal reduction due to shadowing of El sensing area. (a) Odd interlace, Device 'C'; (b) Even interlace, Device C'; (c) Odd interlace for redesigned version, Device 'B'; (d) Even interlace, device 'B'
Master Clock frequency = 200 KHz



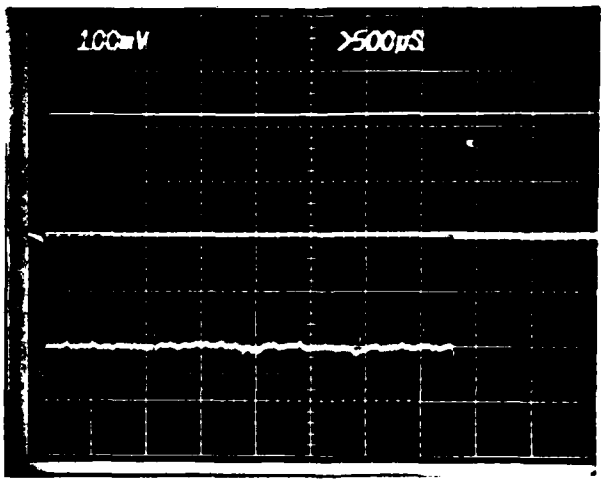
W66A-HSA
$\emptyset_R$ = 25 V

(a)



W66A-HSA
$\emptyset_R$ = 15 V

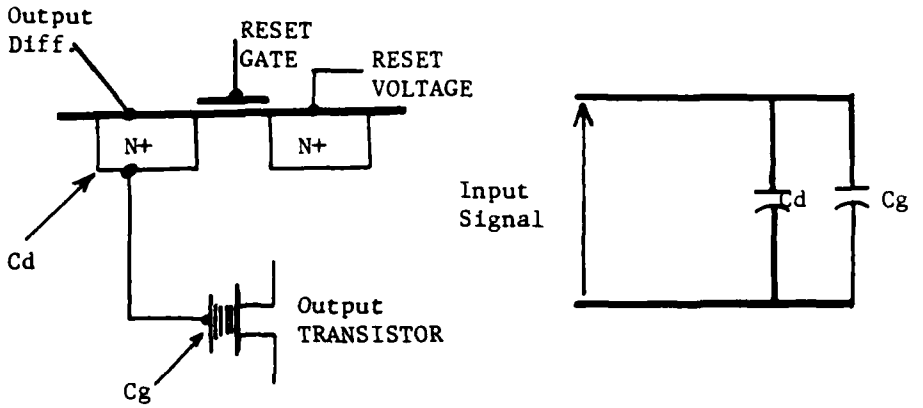
(b)



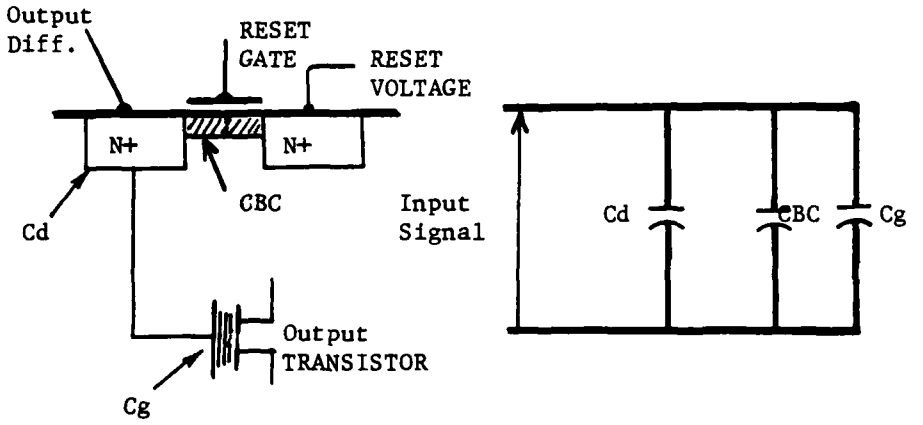
W66A-HSB
ØR = 15 V

(c)

FIGURE 10: Output video level for the A and B devices under same input light conditions.



(a)



(b)

FIGURE 11: Output charge sensing circuit (a) with enhancement reset transistor, (b) with depletion reset transistor. An additional capacitance saddles the output node in (b) reducing the effective voltage signal on the output transistor for equivalent signal change.

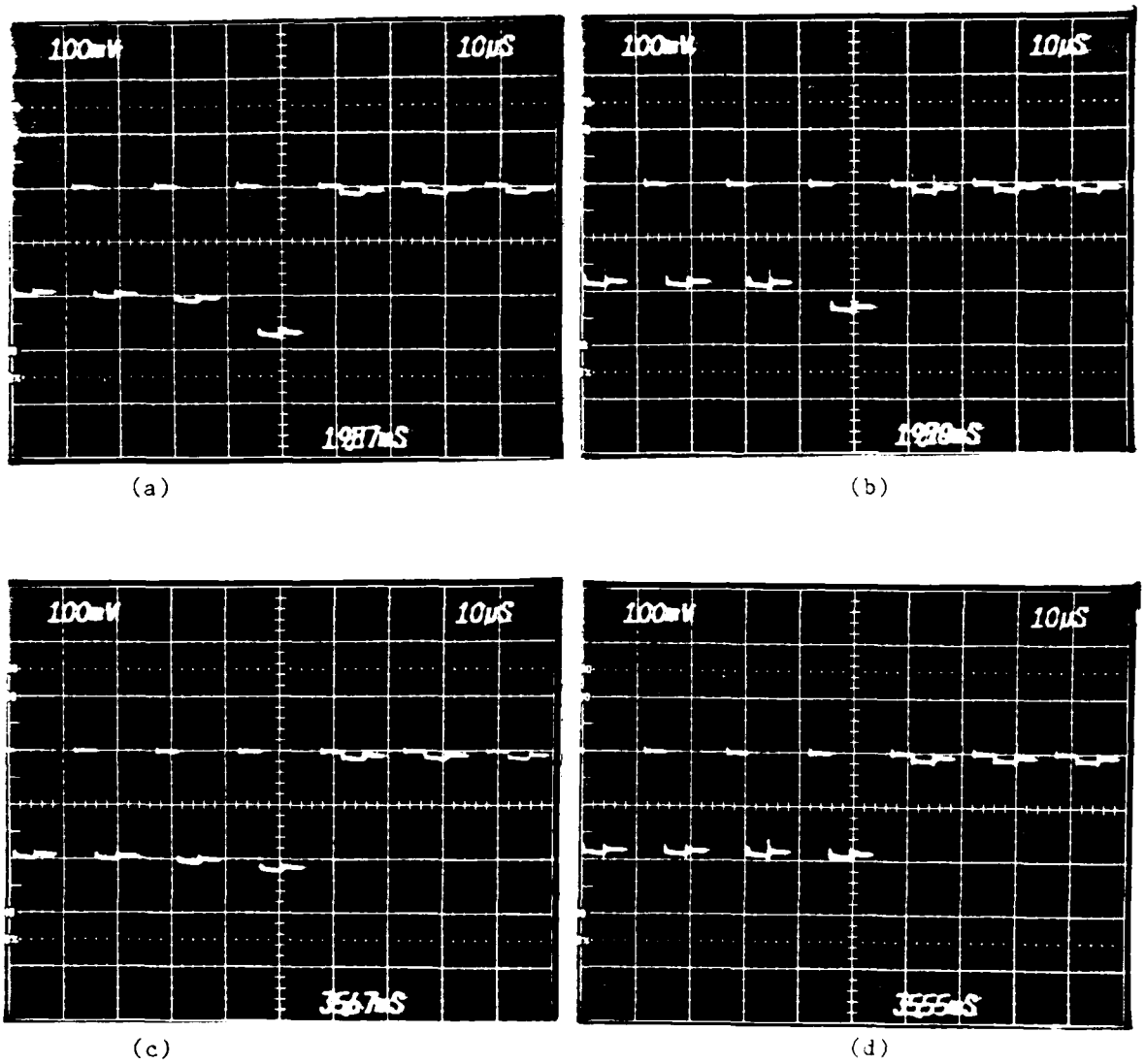


FIGURE 12: Photograph shows excess signal in input-end and output-end pixels, before and after cutting for device G3, W66A-HSA
(a) Pixel #1 before cutting; (b) same as (a) after cutting;
(c) Pixel #2 before cutting; (d) same as (c) after cutting.

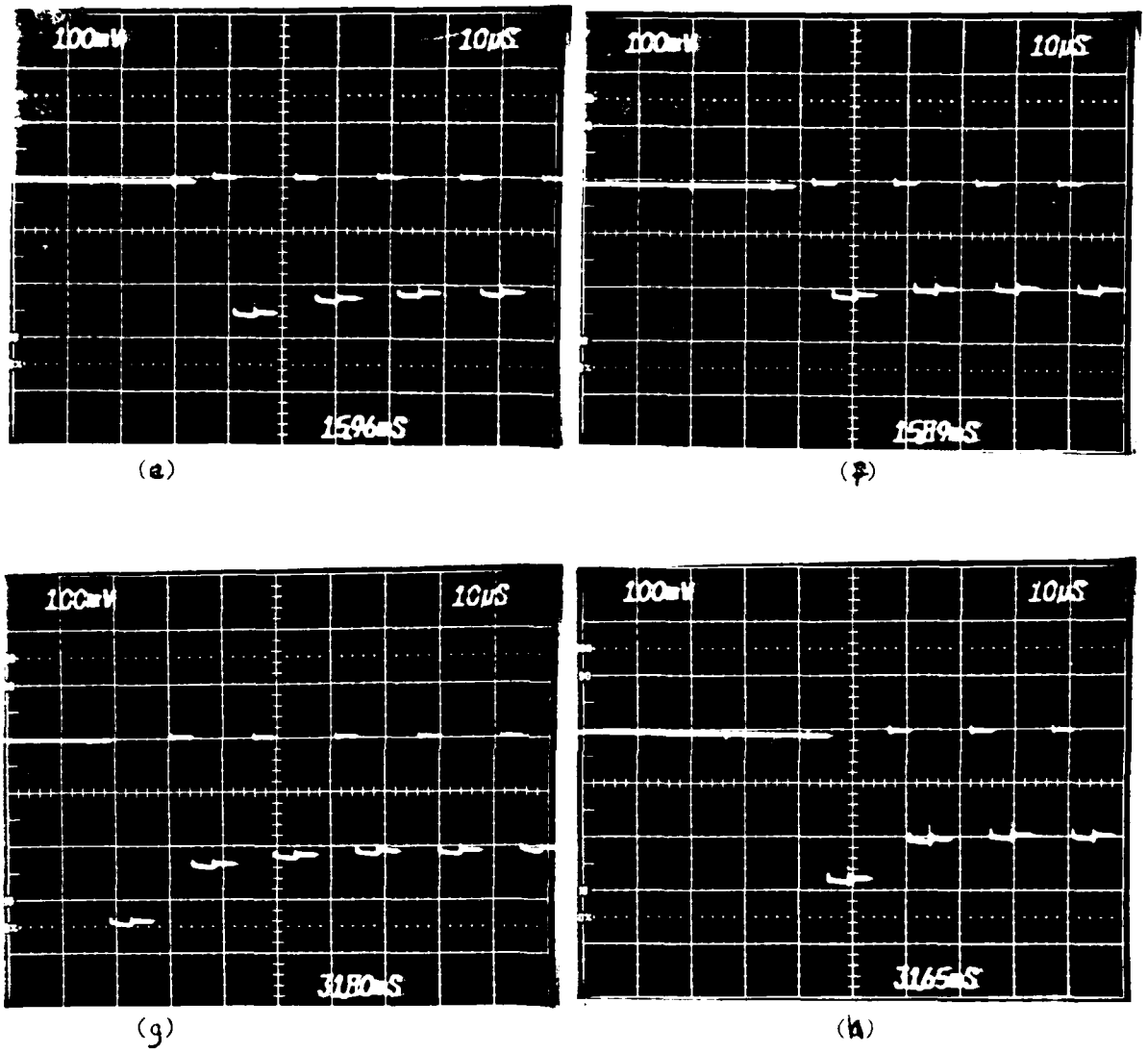
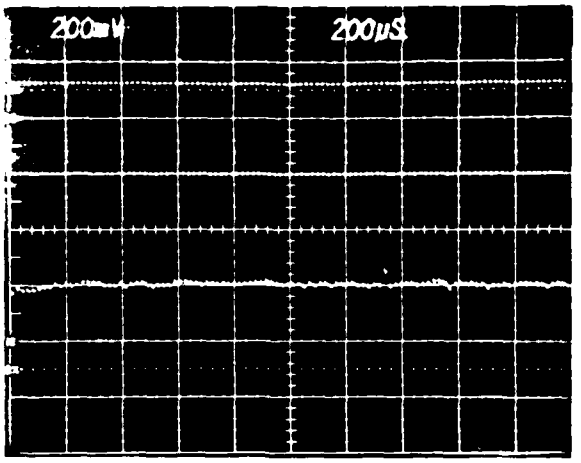


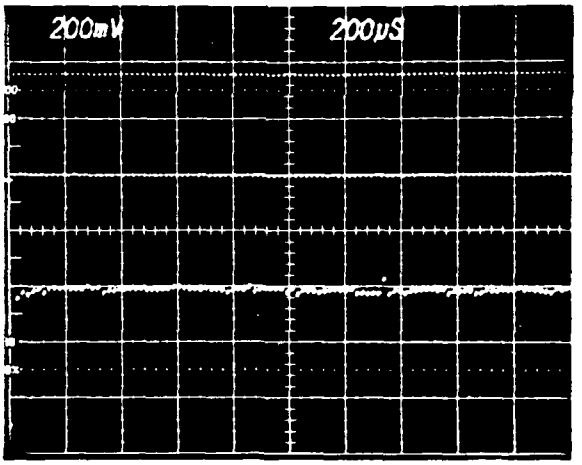
FIGURE 12 (Cont'd):
(e) Pixel #2047 before cutting; (f) Same as (e), after cutting;
(g) Pixel #2048 before cutting; (h) Same as (g), after cutting.

(a)



395 mV

(b)



415 mV

FIGURE 13: Output signal level for W66A-HSB device.
(a) Mid-tap output
(b) End-tap output

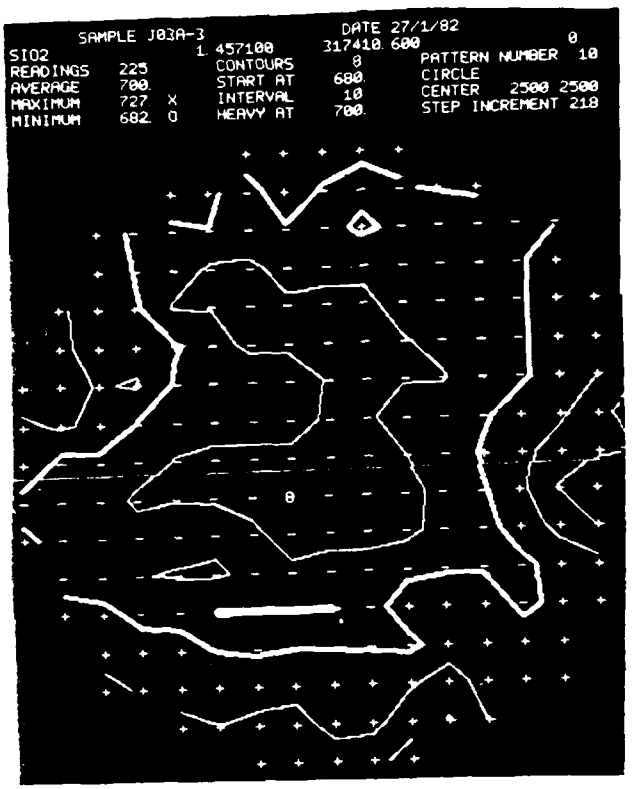


FIGURE 14: Thickness contours of the 700 Å thermal SiO_2 layer

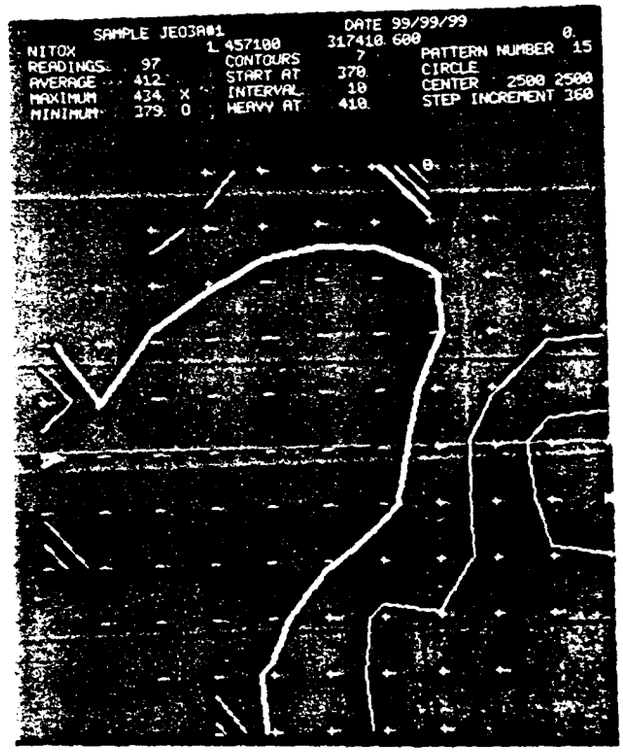


FIGURE 15: Thickness contours of the 400 Å silicon nitride layer

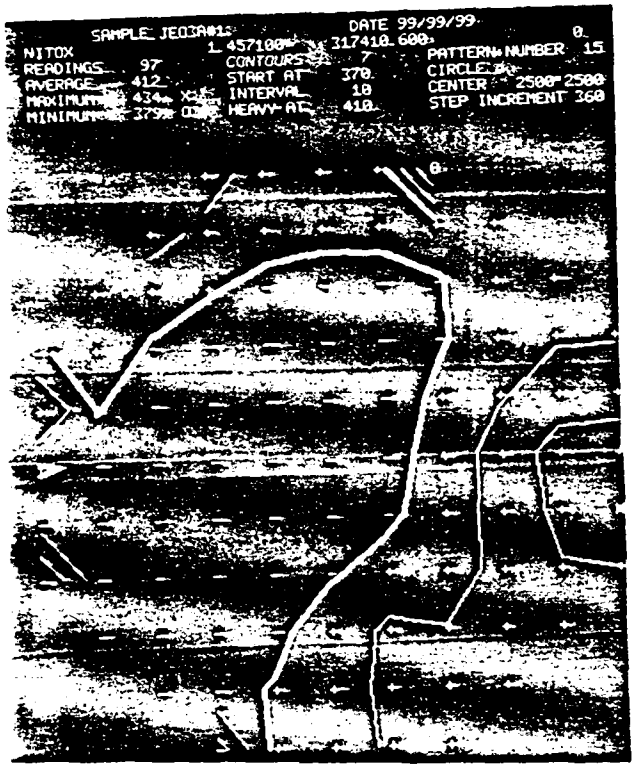
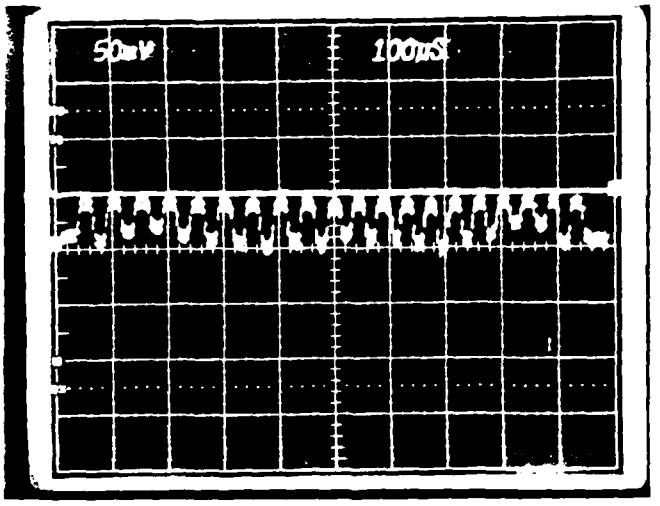


FIGURE 15: Thickness contours of the 400 Å silicon nitride layer

(a)



(b)

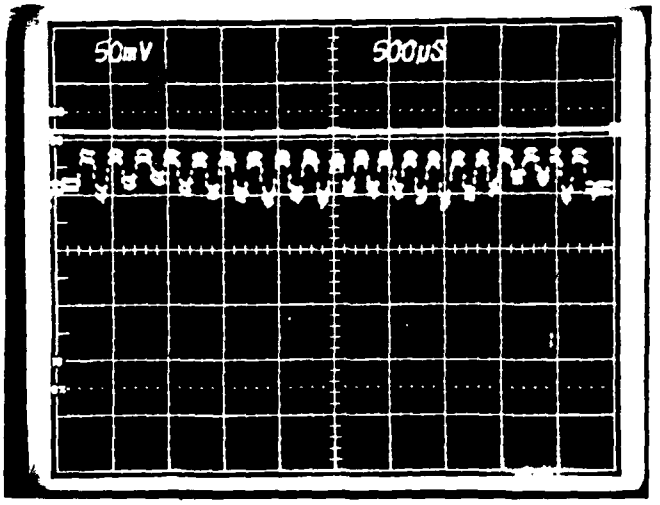


FIGURE 16: Video output for optical input (bar pattern) for a master clock frequency of (a) 1 MHz, (b) 260 KHz

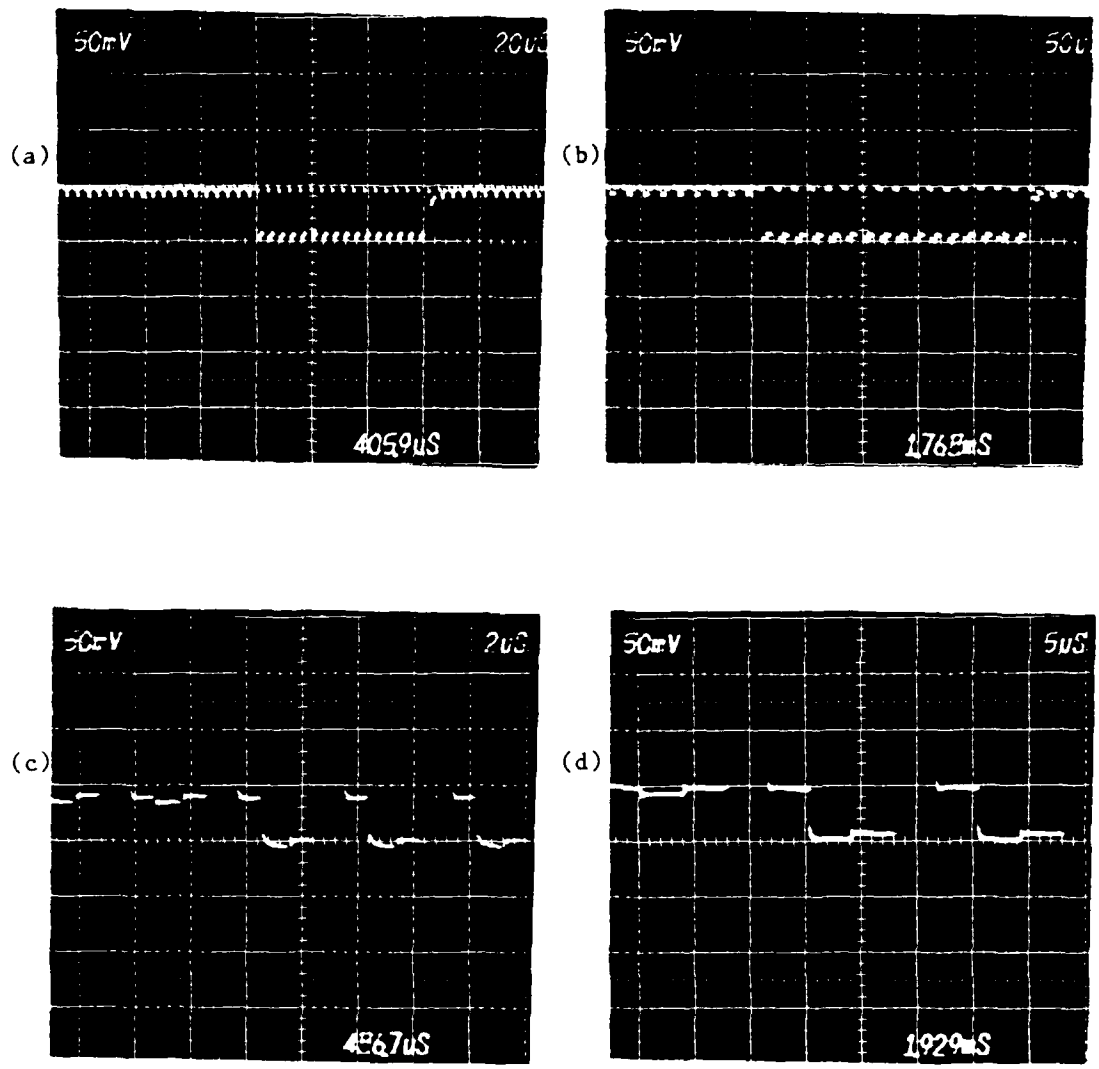


FIGURE 17: Video output (end tap) of electrical input, using a fill-and-spill technique, with a master clock frequency of (a) 1 MHz and (b) 260 KHz.

(c) and (d) are expanded versions of (a) and (b) respectively.

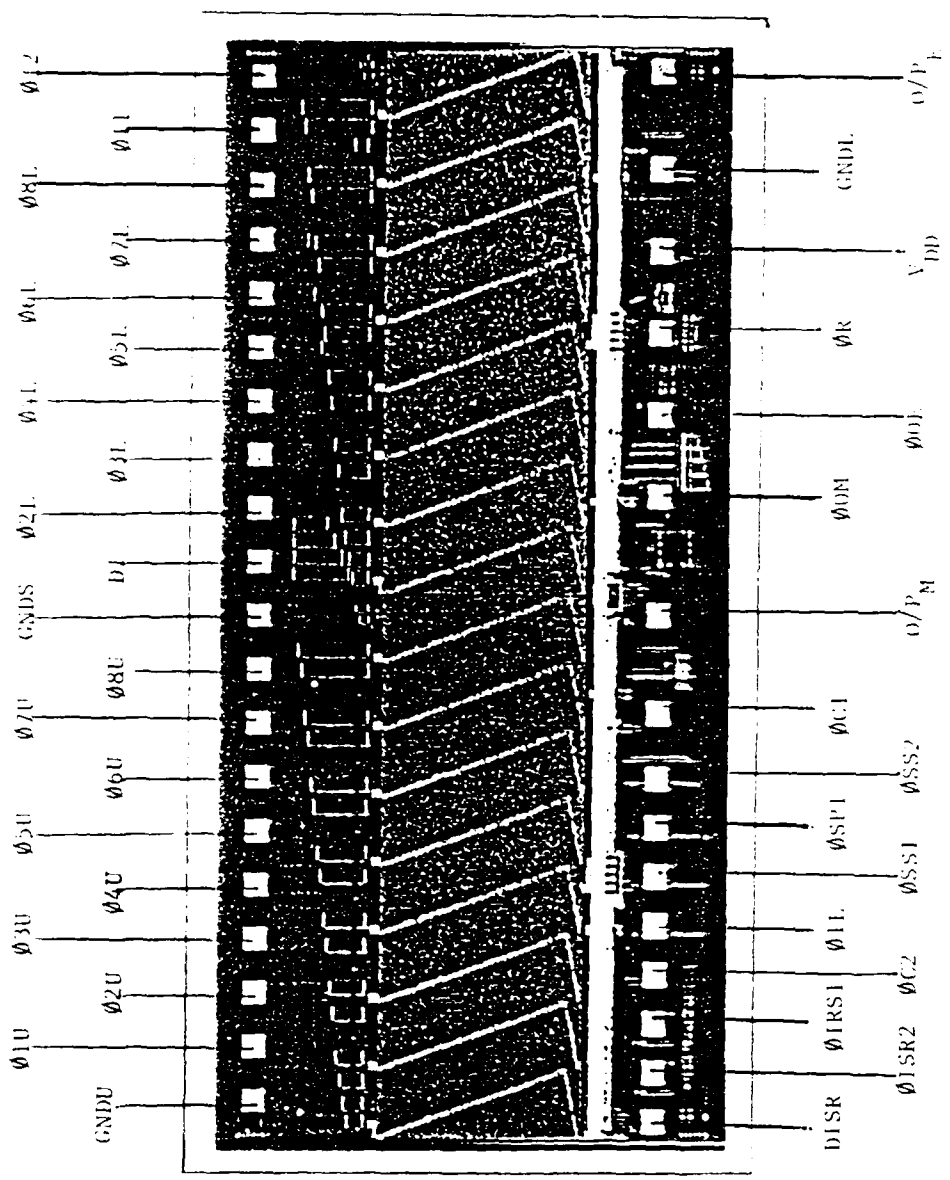


FIGURE 18. Bonding Pad Description of W62A

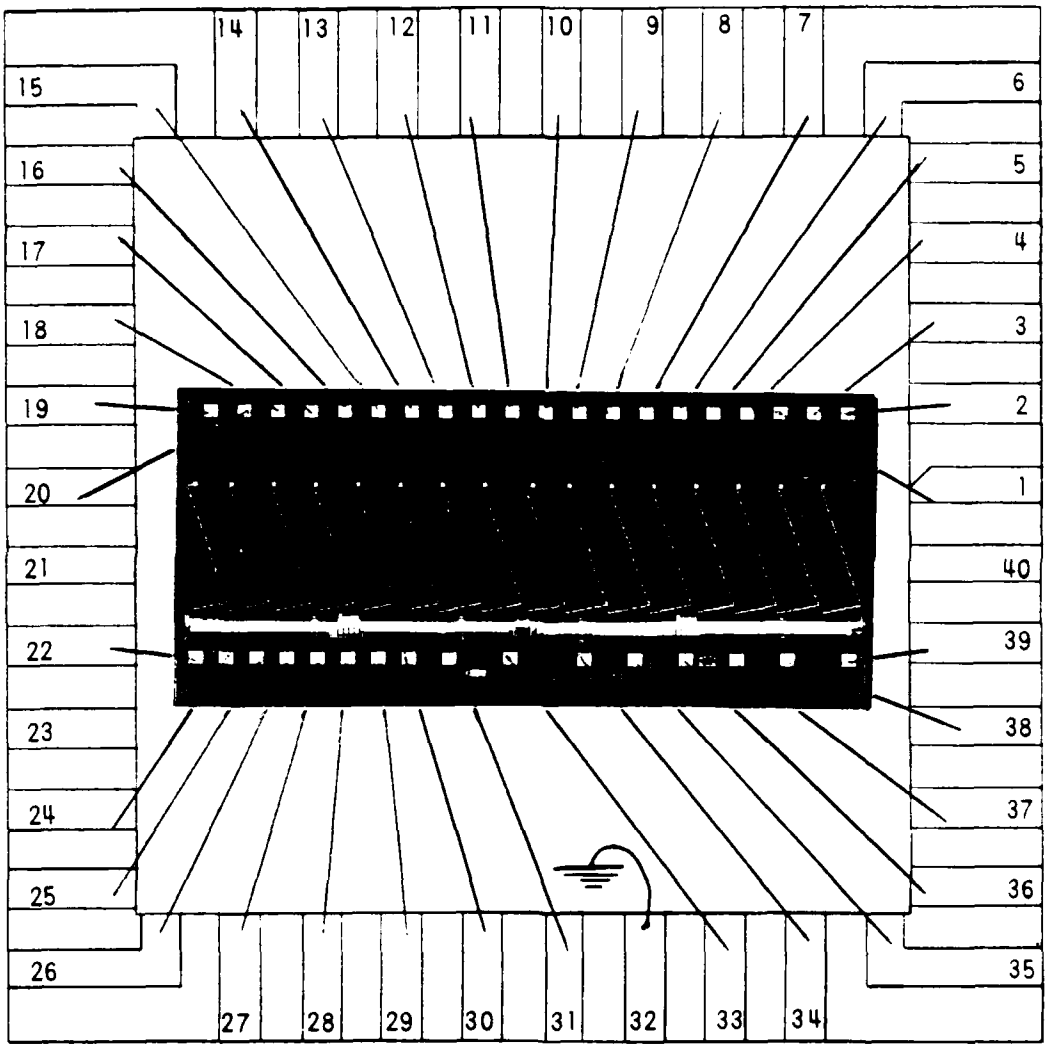


FIGURE 19: Bonding Diagram of W62A

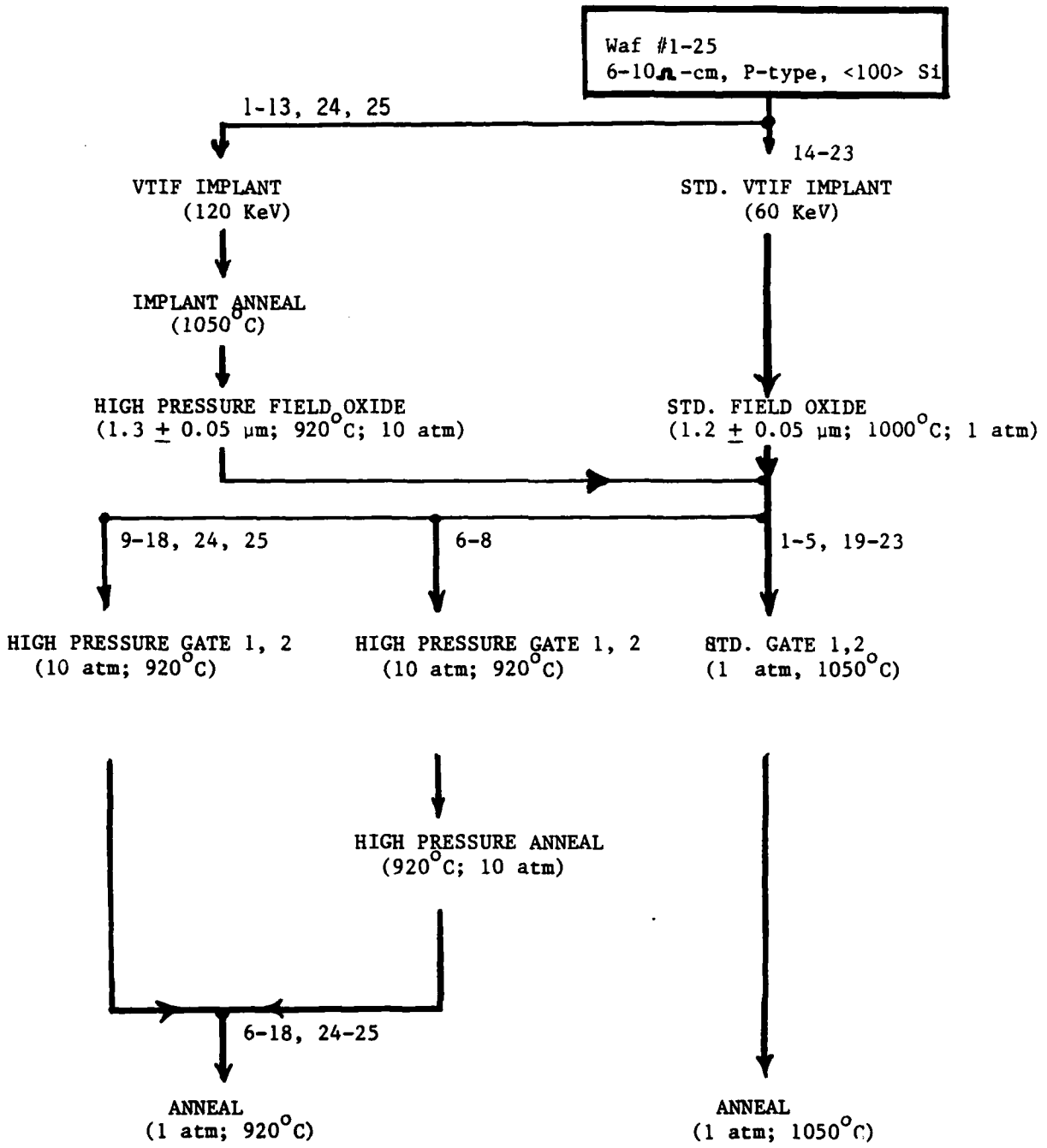
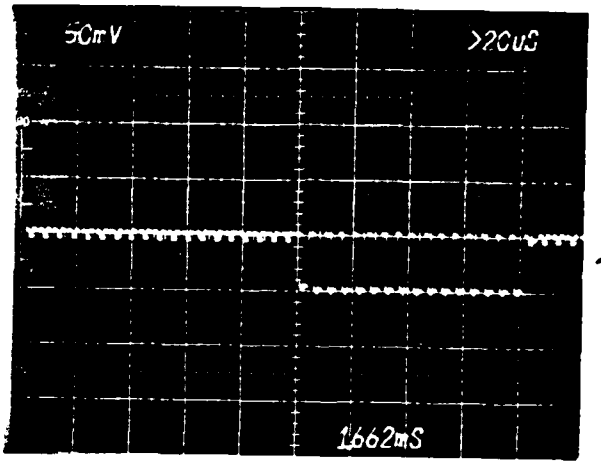


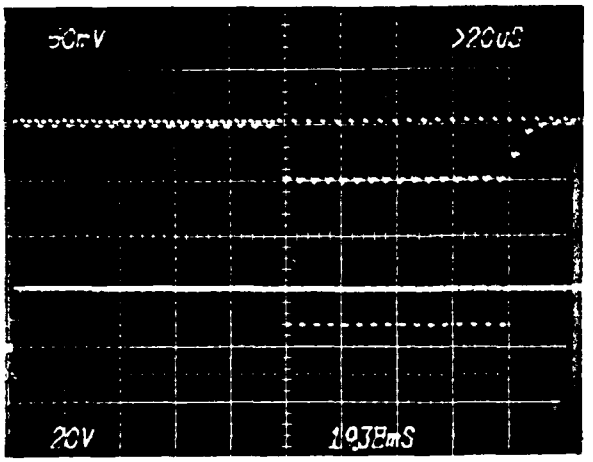
FIGURE 20: Process matrix for Batch JE08B

(a)



S/R OUTPUT

(b)



S/R OUTPUT

INPUT
SIGNAL
(1s "ONES")

FIGURE 21: Shift register output for an electrical input of a string of 16 "ones", (Diode input; fill-and-spill technique).
Clock voltages (a) 22V; (b) 18V
[Batch JE08B, WAFER #10; MASTER CLOCK FREQUENCY = 400 KHz]

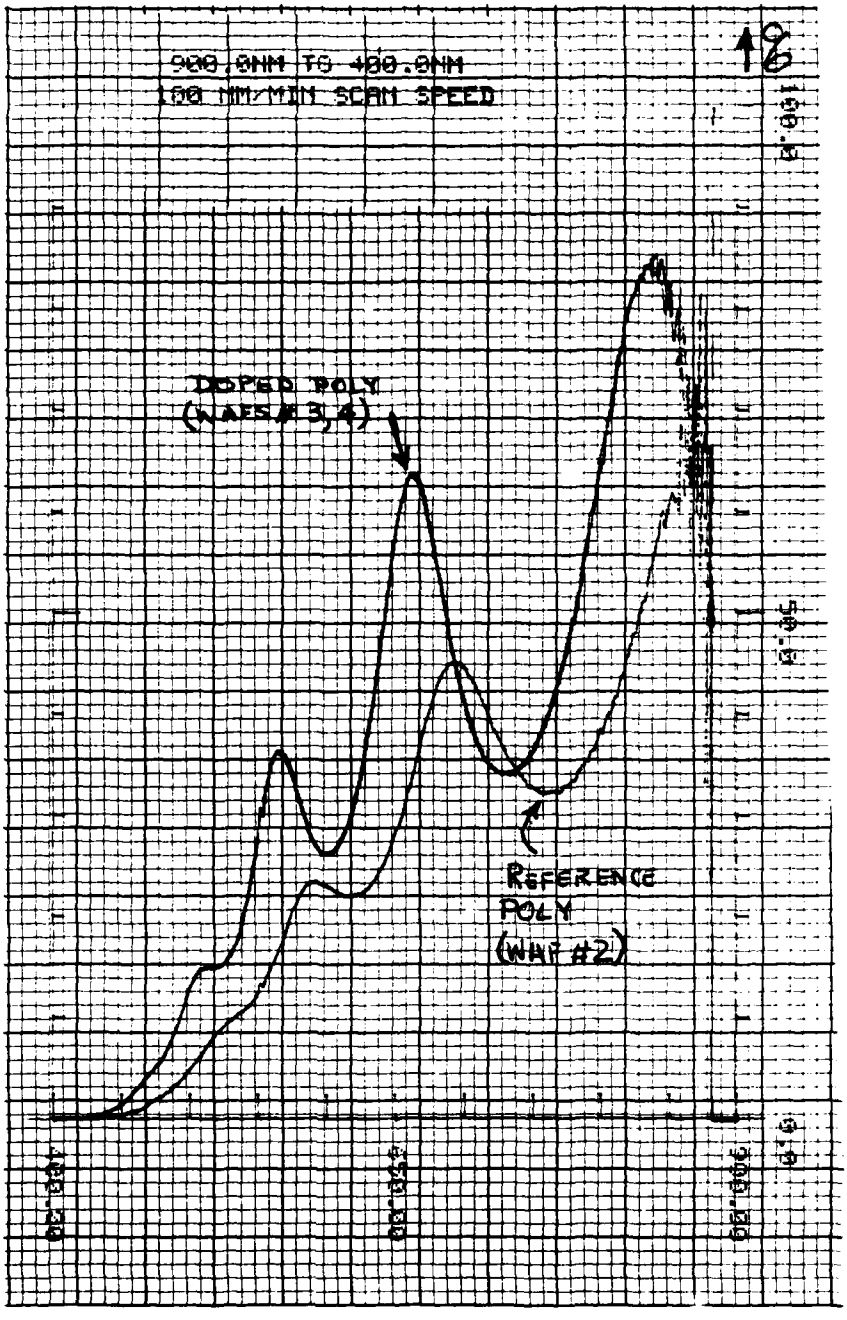


FIGURE 22: Optical transmission characteristics for doped (in situ) polysilicon (3300 Å) and reference undoped polysilicon (3550 Å). Uniformity of spectral response for doped Wafers #3, 4 is evident since the two graphs coincide.

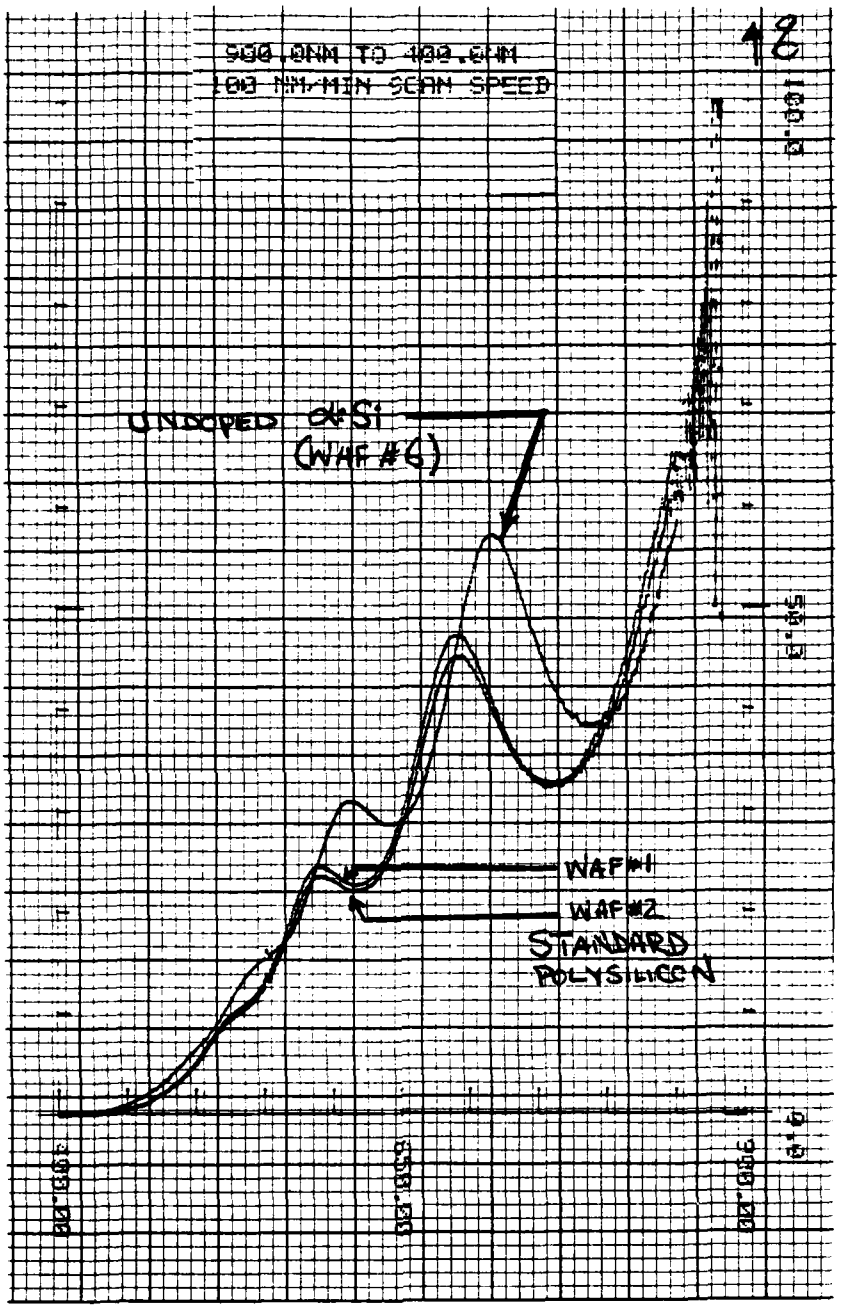


FIGURE 23: Optical transmission characteristics for amorphous silicon (Wafer #6), 3600 A° thick, and standard undoped polysilicon, 3600 Å thick (Wafer #1, 2). Note the slight difference in uniformity of spectral response for the standard polysilicon layers.

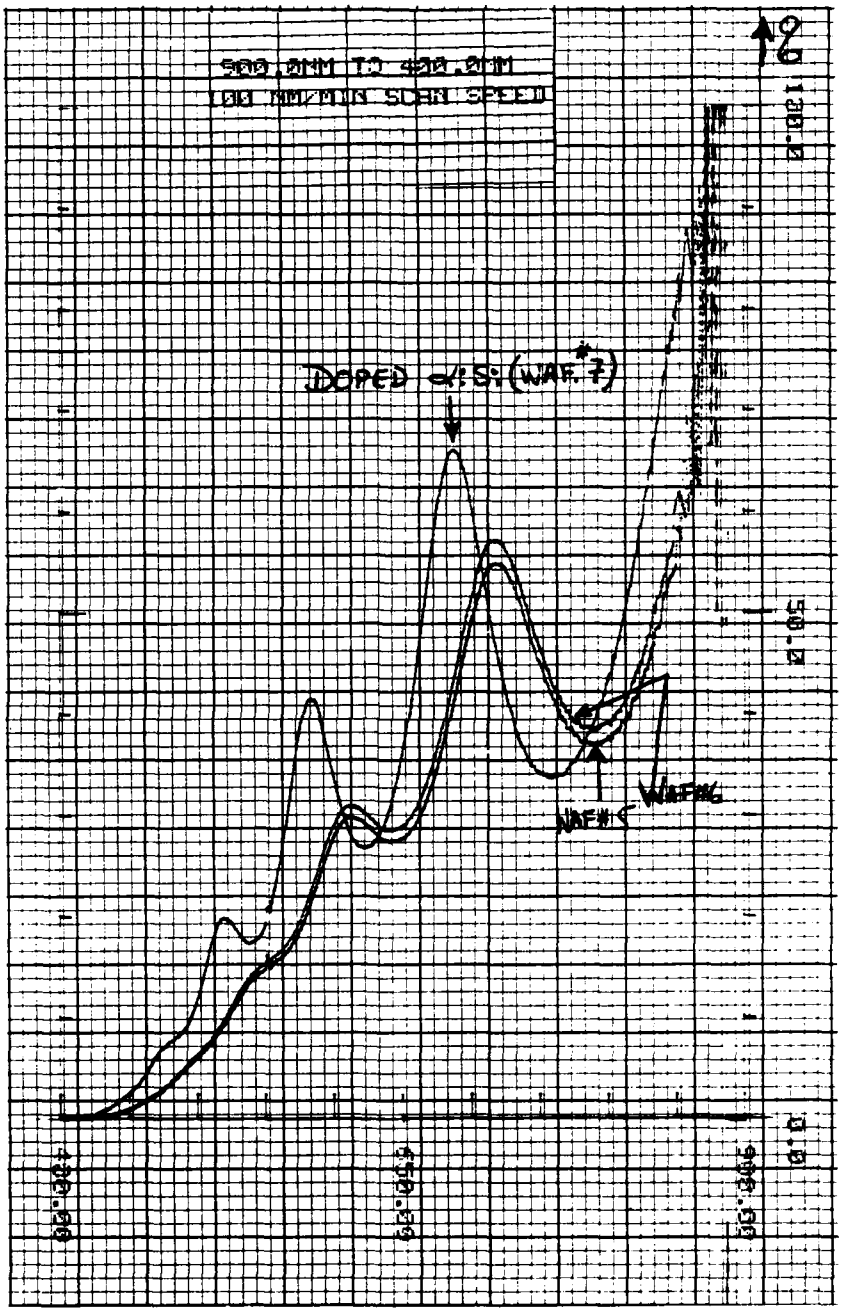


FIGURE 24: Optical transmission characteristics for in-situ doped (Wafer #7) and undoped amorphous silicon (Wafer #5, 6).

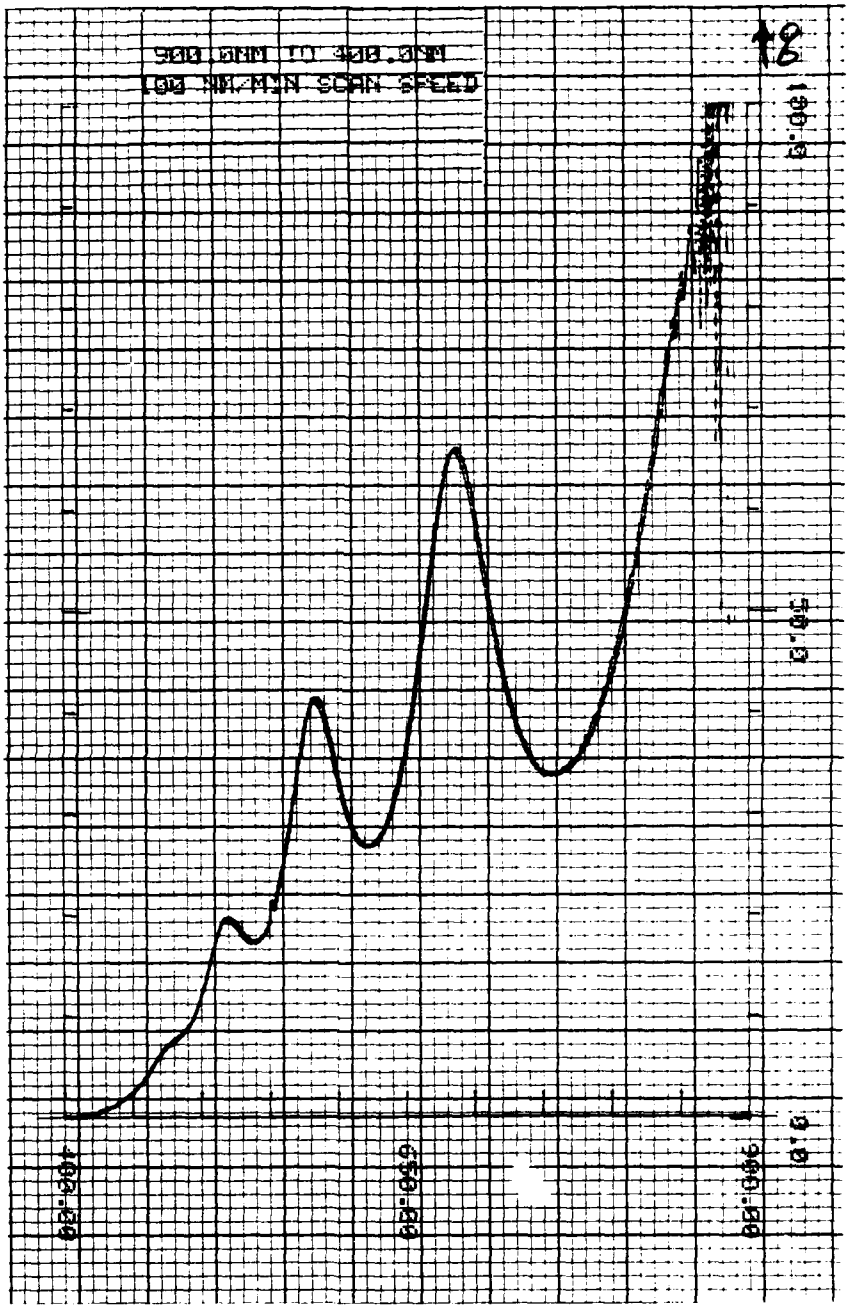


FIGURE 25: Optical transmission uniformity for in-situ doped amorphous silicon (Wafer #7, 8). Note that the two graphs coincide.

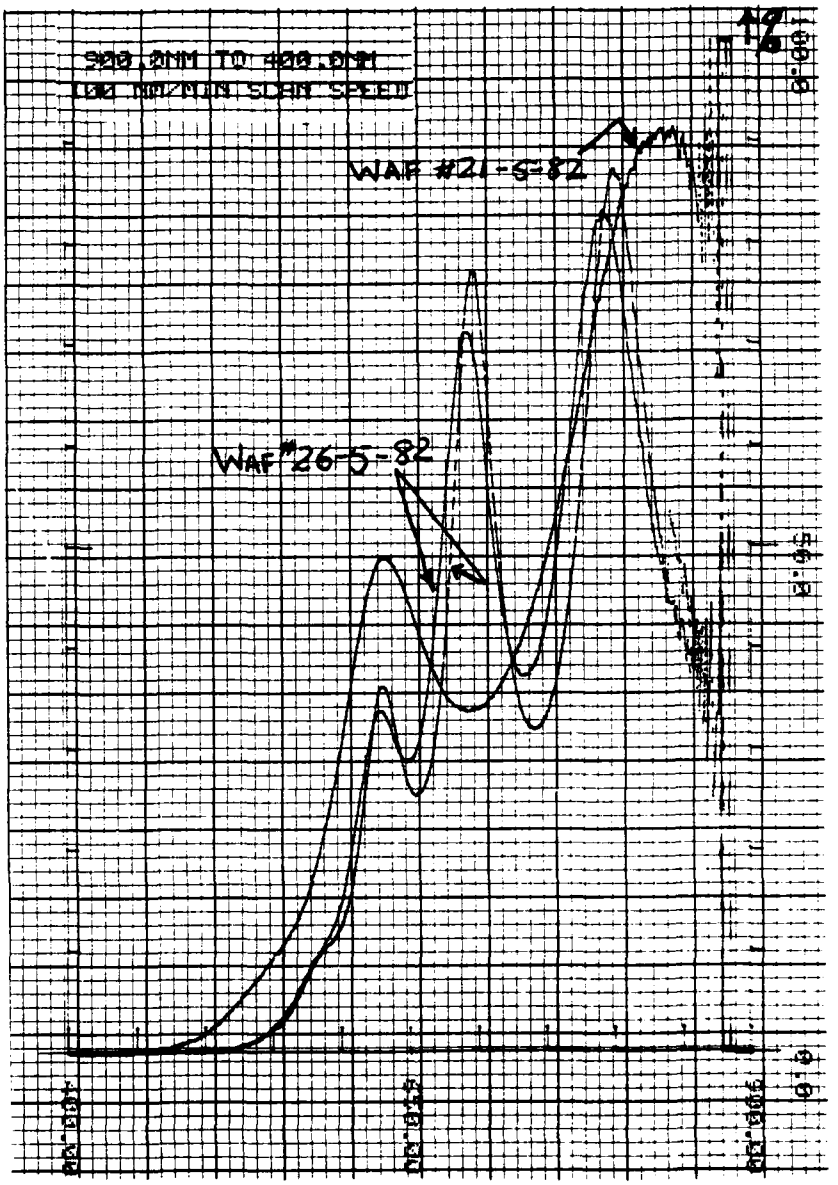


FIGURE 26: Optical transmission characteristics for dc glow discharge hydrogenated amorphous silicon samples (3500 Å). Wafer #26-5-82 is measured at two different places on the same sample.

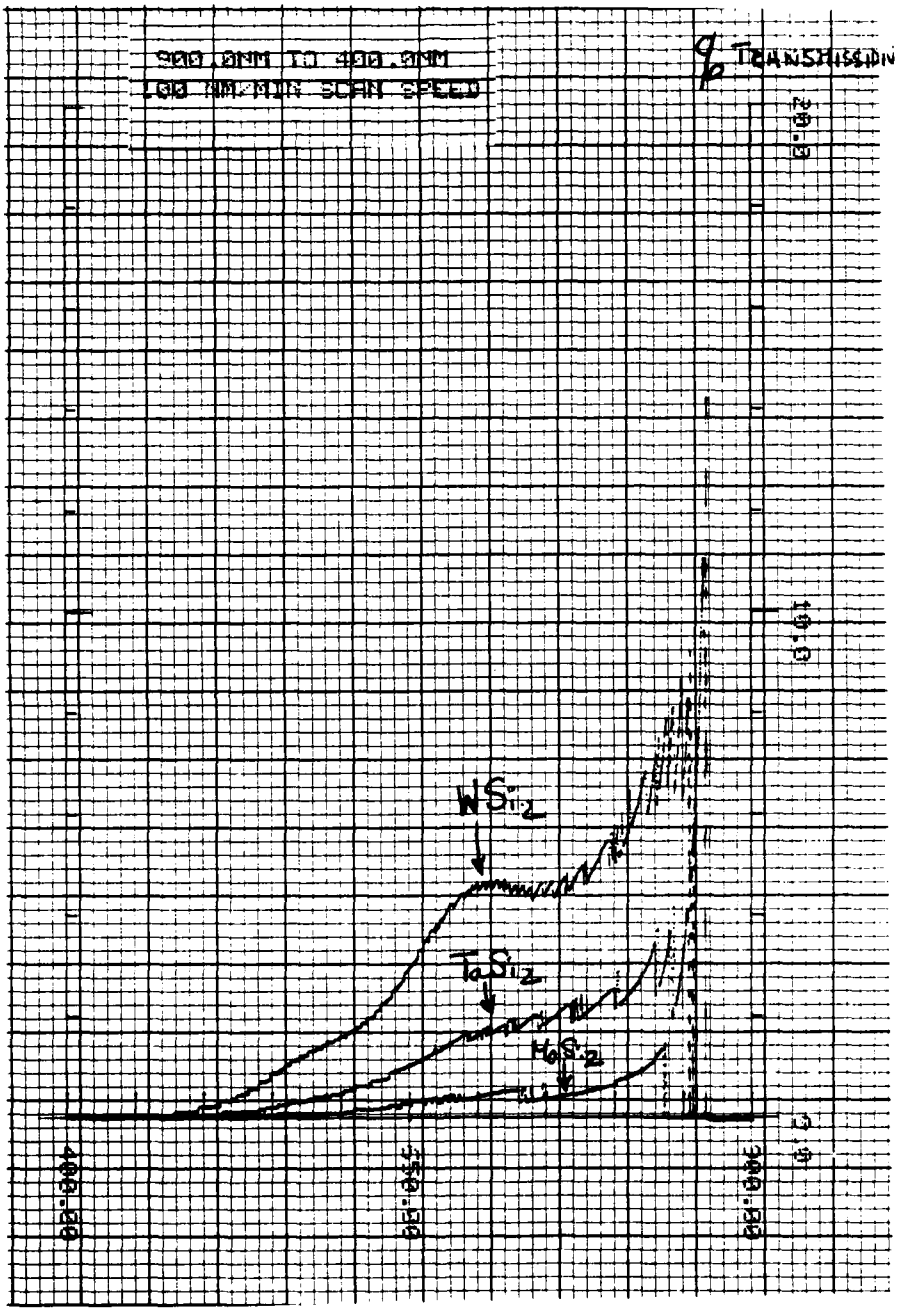


FIGURE 27: Optical transmission characteristics of 500 Å thick silicide on 3000 Å polysilicon.

15. APPENDIX I

Introduction

The W66A is a monolithic charge coupled imager test chip designed specifically for the evaluation of new design and fabrication approaches aimed at improving device performance, reliability and yield of buttable, time delay and integration (TDI) imagers. It is fabricated with the BNR double polysilicon, double metal, buried-channel CCD technology.

A continuous array can be formed by mounting edge buttable CCD imager chips side-by-side with all connections made through the non-buttable side of the chip. With this approach, a very long focal plane array can be formed without being limited by the physical length of an imager chip.

The time delay and integration mode of operation is necessary in certain imaging applications where there is a large linear motion, with respect to the focal plane, of the scenery to be imaged during the integration period. In this mode of operation, the line imagery formed from a scene is clocked from a linear array to an adjacent linear array to compensate for the image motion. The effective exposure time can thus be increased many times over that of a linear array without causing smearing in the imagery. The time delay and integration mode of operation provides superior signal-to-noise ratio and is particularly useful for low light level imaging applications.

General Description

Based on our previous experience in buttable, time delay and integration imager development, areas requiring exploratory design and fabrication work were identified and formulated. Since a risk of lower yield exists with some of the redesign schemes, implementation of all these design features on a single heavily redesigned chip is not recommended. The approach taken here is to include three, nearly identical, TDI arrays on the chip as test vehicles. Each of these will be dedicated to a selected set of redesign schemes. The first array is a reference array with all design features unchanged from the 2048 x 96 TDI device. This array is used to identify and

isolate problems other than those resulting from design changes. The second and third arrays share the design iterations. With this approach, better device yield is expected to be obtained and individual design and fabrication problems can be investigated without ambiguity.

The organization of W66A is shown in Figure 1. The size of the chip measures 370 x 356 mil^2 and is divided into six sections. The three large sections designated W66A-HSA, W66A-HSB, W66A-HSC on the left hand side of the chip each contain a 96 x 512 element TDI array. These three TDI arrays share the same design architecture. The differing design features on each array will be discussed in the following section. The three smaller sections, all designated W66A-HSZ, on the right hand side of the chip are the BNR test inserts. They contain a number of test structures for device analysis and process parameter monitoring.

Owing to the small geometry and large die size involved, fabrication and maintenance of mask sets for large area TDI imagers has historically consumed a large part of the fabrication effort. For example, the mask of our one inch long, 96 x 2048 element E57B TDI imager was fabricated by photo-composition of eight patches of data in the form of reticles. The master plates and working copies were then generated from the reticles. The stringent requirement on defect density usually resulted in heavy rejection of the working copies during mask making. The good working copies require tedious routine maintenance to ensure the mask is clean and not producing additional defects. This together with the inevitable wear-out of mask plates during contact printing makes mask making and maintenance both laborious and expensive. Future technology trends requiring smaller pixel size and large pixel number on a chip would impose further difficulties on standard mask making approaches. Therefore, more advanced photolithography techniques are examined for easier and better pattern definition. The availability of the GCA4800 direct wafer stepper in BNR makes it an attractive choice for photolithograpy. The superior alignment accuracy and image resolution of the wafer stepper is particularly favourable for patterning fine overlapping polysilicon structures for CCD's. The non-

contact printing method used for the wafer stepper also will eliminate mask wear problems. Device patterning using the GCA4800 can be done directly from the reticle without the necessity of generating master and working copies of the mask. This greatly reduces the number of masks required for patterning and will result in a significant reduction in the cost of mask making, the cost of mask maintenance and the turn around time of mask making.

The mask set of W66A is designed for the wafer stepper operation. A special set of alignment marks is included on the chip to make it wafer stepper compatible.

The mask set is also designed to exploit the superior properties of positive resist over negative resist. Recent work at BNR has demonstrated that positive resist has better pattern transfer characteristics and higher resolution performance than currently available negative resist systems.

Individual Array Description

W66A-HSA

The W66A-HSA is a 96 x 512 element TDI CCD imager, the organization of which is shown in Figure 2. The same organization is used for W66A-HSB and W66A-HSC. The W66A has 512 elements in the horizontal direction and 96 elements in the vertical (TDI) direction. The pixel size is 13 x 13 um^2. The chip consists of an electrical input to the TDI imaging area, a parallel to serial transfer interface for interlaced data output, a horizontal serial shift register, an electrical input to the shift register with file-and-spill input method, an externally selectable, destructive readout tap at the 256th element and a destructive end-output at the 512th element. The horizontal shift register employs two phase clocking while the vertical TDI columns employ eight phase ripple clocking. All the electrical connections to the chip are made through the long, non-buttable sides of the chip so that the active circuits can reach close to the buttable edges. This

architecture minimizes the optical dead space between chips when they are butted together.

The major design iteration on this TDI array are:

(i) buttable edge redesign

(ii) input protection device addition

(iii) mid and end output circuitry redesign to remove the split video output level as observed on the E57B imager.

The redesign of the mid and end output circuitry has been implemented and verified elsewhere (W62A) [reference 1] so this part of the redesign is relatively straight forward.

The addition of input protection devices to the chip was found to be necessary to prevent destructive failure during separation and handling of devices. Electrostatic discharge problems were observed repeatly on some earlier designs especially during die sawing. A heavy die loss of unprotected devices was often incurred even when stringent handling precautions were taken.

The most important design iteration on W66A-HSA is the redesign of the circuitry at the, already densely packed, buttable edges. In order to minimize the gap between two adjacent chips, tight geometries, which violate the conventional design rules, were employed. In order to be able to use chemical etching techniques in the fabrication of buttable edges to tighter tolerances, extra room for a n+ diffusion guard-band at the chip edge is required [reference 2]. A new design which allows the insertion of 3 um n+ diffusion at each buttable edge while maintaining 2 pixel gap between adjacent chips is shown in Figure 3. The new design abandons the symmetry concept used (i.e., the distance between the butt edge to the center of the outermost pixel being equal on both buttable edges). Instead, the left and

right buttable edge layouts are independently optimized to achieve a minimum overall gap between chips. The insertion of a minimum 3 um wide n+ guard band was found to be necessary to prevent charge injection into the active circuit from the chip boundary. An optional silicon nitride mask layer has also been designed to define the physical position of the buttable edge when anisotropic chemical etching is employed. This extra mask allows the physical buttable edge to be fabricated at a predetermined distance between 0 to 8 um away from the design chip edge. The nitride mask will allow the optimum distance between the physical buttable edge to the design chip edge to be evaluated.

W66A-HSB

The major redesign features on W66A-HSB are:

(i) redundant bonding pads

(ii) addition of input protection device

(iii) redesign of the mid and end output circuitry to remove the split video level effect

(iv) reduction of $\emptyset_{1L}$ electrode shadowing

(v) reduction of $\emptyset_R$ reset voltage

(vi) equalization of E1 mode optical sensitivity with the other TDI electrodes.

The design approaches are:

(i) Redundant bond pad area - The design approach is to place one-piece, oversized bond pads instead of two, interconnected, pads. This gives the maximum contact area for a given space. Recommended pad size is 140 um x 250 um.

(ii) Addition of input protection device - The design approach is to use a standard protection circuit based on an RC network with associated diode shunts to protect devices from electrostatic discharge problems.

(iii) Redesign of the mid and end output - The mid and end output circuits are redesigned to remove the split video effect. The design approach taken here is to remove $\emptyset C_1$ capacitive coupling to the output node as implemented on the W62A.

(iv) Reduction of shadowing by $\emptyset_{1L}$ connection - The design approach is to reduce the Poly 2 connection tab from 12 um to 5 um.

(v) Reduction of the high (25V) reset voltage - The design approach is to replace the enhancement mode reset transistor with a depletion device. The reset voltage should then be about 18V. This is a reversion to the 735 reset scheme and has been well verified.

(vi) Equalization of the E1 mode optical sensitivity - Owing to the structural difference between the E1 electrode and the other TDI electrodes, equalization of the E1 optical sensitivity with the other TDI electrodes is best done by slightly reducing the optical window size of E1 electrodes.

It was decided to set the E1 electrode width to 12.5 um instead of 13 um to compensate for variation in optical sensitivity due to structural differences.

W66A-HSC

This is the reference device. The array employs all the standard design techniques of previous BNR TDI imagers.


DAT
FILM